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RESEARCH ARTICLE

DESIGN OF THE TIME HOPPING SPREAD SPECTRUM SYSTEM BASED ON FPGA

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ARTICLE INFO	ABSTRACT
Article History:	General wireless communication system has many shortcomings, for example the poor ability of anti-
Received 16 th August, 2015 Received in revised form 24 th September, 2015 Accented 23 ^{td} October, 2015	interference, anti-jamming and anti-multipath performance. In this paper proposes, a design of time hopping spread spectrum system based on FPGA is proposed. When sending information code, the pseudo random code is used to control the on-off switch to send the information data of storage by the jumping order and achieve the time sequence of jump in the sending end. In the receiver, the local pseudo random

interference, anti-jamming and anti-multipath performance. In this paper proposes, a design of time hopping spread spectrum system based on FPGA is proposed. When sending information code, the pseudo random code is used to control the on-off switch to send the information data of storage by the jumping order and achieve the time sequence of jump in the sending end. In the receiver, the local pseudo random sequence is used to control local on-off switch to realize the solution of the modulated data after capturing the sync signal and restore the original information data. Both Verilog HDL and principle diagram method are employed to design the circuit in the Alteral company Quartus II software. The system of design is realized on FPGA.

Key words:

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Time Hopping; pn code; Modulation; Demodulation; FPG₁

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INTRODUCTION

With the rapid development of a series of innovative and high technology, the accuracy and safety of the signal in the field of military and civilian communications are becoming higher and higher. Spread spectrum communication system has good performance of anti-jamming, anti multipath fading, high precision measurement, multiple access, and other excellent performance, for many years has been rapid development and wide used [1]. TH (Hopping) is similar to the frequency hopping (Time), which makes the transmitted signal jump on the time axis. First, the time axis is divided into many pieces, in a frame, the signal is controlled by a spreading code sequence. Can be understood as: Time shift keying with a certain code sequence to select the time slice.

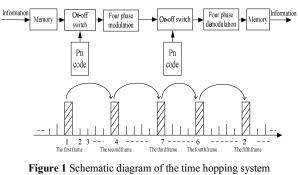
As a result of the use of a lot of time to send a signal to send a lot of time, relative to say, the spectrum of the signal is also broadened [2] Spread spectrum communication systems usually use the microprocessor and digital logic unit to design, but the processing speed is slow, available logic resources are limited, and is not easy to simulate and other factors limit the spread spectrum communication system design and development [3]. With the development of programmable logic device, FPGA technology has become more sophisticated, internal logic is rich in resources, Nios II soft core processing ability is stronger, simulation ability is stronger, repeat programming, on-site can modify the design, the corresponding EDA (Electronic Design Automation) software function perfect, rich IP (intellectual property) core resources and so many advantages [4], which makes FPGA has become the first choice for the design of spread spectrum communication system.

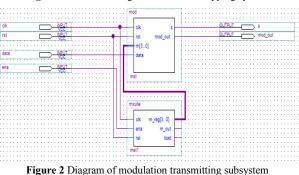
The principle of the spread spectrum system

Time hopping spread spectrum code control system is the use of jump information symbols in the time axis, the chip uses a narrow lot to send signals, relatively speaking, the frequency spectrum of the signal is expanded. Figure 1 is a time hopping system principle diagram. In the transmitter, the input data stored, generated by the spread spectrum code generator spreading code sequence to control the on-off switch, the phase or four phase modulation, then by RF modulated emission. In the receiving terminal, the output of the intermediate frequency signal which is produced by the RF receiver is controlled by the same spreading code sequence as the same as the originator, and then the second phase or four phase demodulator is sent to the data storage data [5]. As long as the sending and receiving ends strictly on time synchronization, can accurately recover the original data.

General system formula

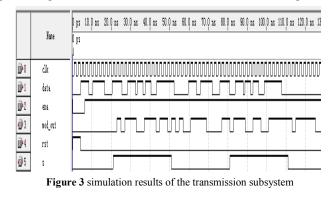
In the transmission system, the data stored in the memory is stored in the memory, and the 15 kinds of random sequences generated by the 4 bit PN codes are used to control the on-off switch, to jump to read the stored information data and get modulation output mod_out, sending the spread spectrum. In the receiving system, the synchronization module is captured by the synchronous signal, the local PN code control switch to the information data to receive the jump, get the solution to expand output emod_out. Comparison of emod_out with the sending end of the data information data the waveform map, so as to verify the design of the time spreading system correctness and feasibility.





System modular design

Based on the system design scheme, the system can be divided into sending subsystems and receiving subsystems. PN code generation module and storage module is needed in the transmission subsystem. In the receiving subsystem, the synchronization signal capture module, the local PN code generating module and the demodulation module are required.



Sending subsystems

The modulation transmission subsystem, mxulie module for the 4 bit PN code generator module, 15 kinds of pseudo random sequence, used to control the on-off switch. The mod module for storage, modulation module, in which 15 data storage unit,

mainly to complete data storage and time hopping modulation. Input terminal data for information data input. The output terminal mod_out is the modulation output, the S is the storage state change cycle. From the simulation results, it can be seen that the storage state change period is 15 clock cycle, which is in line with the design requirements. Modulation of output mod_out is the input data of time hopping spread spectrum output, realizes the functions of the time hopping spread spectrum function.

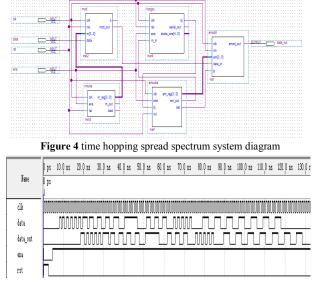


Figure 5 time hopping system simulation results

Receiving subsystems

Figure 4 shows the time hopping spread spectrum system diagram, including the Tongbu module, the emxulie module and the emodd module constitute the receiving subsystem. Tongbu module is a functional module which is used to capture the synchronous signal by sliding correlation, which is strictly controlled by the synchronization between the receiver and the transmitter [6].

The emxulie module is a local pseudo random sequence generation module, which generates a pseudo random sequence for the receiver. The emodd module is the core module of the solution and the expansion of the received signal is obtained by the strict synchronization control.From the design of the hopping system simulation results, compared with the original data, the demodulation output data data_out, has a certain delay in time.

This delay is derived from two aspects, one is the inherent time delay of sequential circuits itself;the other is the time hopping system to send data frames in the wrong time slice, Then, at the receiver despreading, to restore the original data frame time slice and the order will have a certain delay. It can be seen from the diagram that the delay is a nanosecond, and it can be accepted in the general communication system. From the point of view of the waveform, the output data is consistent with the originating data. This is to say, the design of the jump spread spectrum system is correct and feasible.

CONCLUSIONS

This article put forward a design of FPGA based on time hopping spread spectrum system, and using the method of combining the principle diagram and hardware description language Verilog HDL in the Quartus II software platform, give a top-down design and simulation verification to the spread spectrum subsystems of sending and receiving algorithm in the system and subsystem module. Finally through the whole jump spread spectrum system simulation, compare the output data data_out and the origin data data, verify the correctness of the design. To design a good jump when the system implementation in FPGA, the result and simulation result is consistent, further shows the feasibility of the design.

Acknowledgments

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