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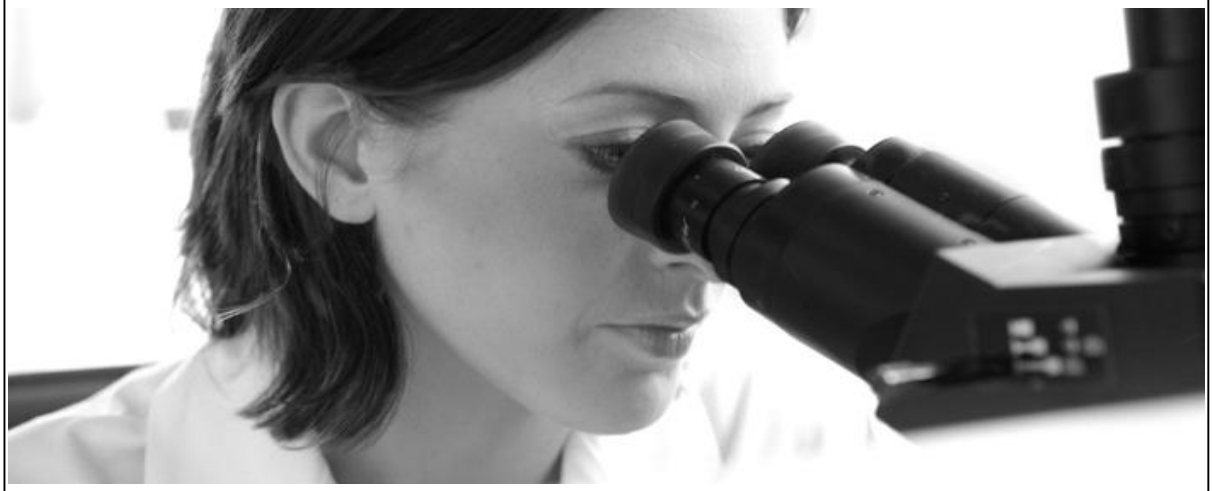

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RESEARCH ARTICLE

IMPLEMENTATION AND PERFORMANCE ANALYSIS OF HIGH-SPEED AND LOW-POWER DIGITAL LOGIC FUNCTIONS BY MULTI-THRESHOLD CMOS (MT-CMOS) USING TANNER EDA

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ABSTRACT

Power dissipation and propagation delay are the major concern in modern CMOS VLSI designs. The reduction of threshold voltage increases the operational speed or computational speed of a digital logic circuit but it unfortunately increase in the sub-threshold leakage current as well and thereby it increases the static power dissipation of a circuit. Multi-threshold CMOS (MT-CMOS) technology provides a convenient solution for this problem, using which both sub-threshold leakage current and propagation delay of a digital logic can be reduced at a time simultaneously without any additional area overhead. Low-threshold voltage MOS transistors are used in the longest propagation path (critical path) to the reduce propagation delay. On the other hand, high threshold voltage MOS transistors are used in the shortest path to reduce the static power dissipation of a digital circuit. The paper describes the implementation and performance analysis of various low-power, high-speed digital logic design methodologies using 2µm technology of TANNER EDA back-end tools.

INTRODUCTION

Power Dissipation and Propagation Delay are the two major key factors for modern high-performance efficient circuit design. In the sub-micron era, supply voltages and threshold voltages for MOSFET are greatly reduced, which reduces the dynamic power dissipation up to certain extent. However, as the threshold voltage of a MOSFET reduces, the leakage current conduction exponentially increases, which in turns increases static power dissipation of a digital logic circuit. Leakage current is a current which flows between Drain and Source of MOSFET when the MOSFET is turned-off. Leakage current depends on SiO_2 thickness between inversion layer and Poly-silicon layer, W/L ratio or "Aspect Ratio" of MOSFET, temperature etc.

However, in a digital circuit, static power dissipation and propagation delay are trade-off. That means, when static power dissipation reduces, unfortunately propagation delay increases and vice-versa. So, the more the threshold voltage of a MOSFET, the more the propagation delay, but the less the static power dissipation. On the other hand, the less the threshold voltage of a MOSFET, the less the propagation delay, but the more the static power dissipation. So, implementing a digital logic which is excellent from all point of view (both less power dissipation & less propagation delay) is somewhat challenging.

So, instead of using ordinary CMOS to implement any digital logic function, implementing the same using Multi-Threshold CMOS (MT-CMOS) is much more convenient to overcome such problem, using which, both Power Dissipation and Propagation Delay of a digital circuit can be reduced at a time simultaneously without any additional area overhead.

Implementation of Digital Logic Using Multi-Threshold Cmos (Mtcmos)

High-speed and low-power digital logic can be implemented using Multi-threshold CMOS technology. MTCMOS technology uses MOSFETs with various threshold voltages – LOW, MEDIUM and HIGH threshold to implement any digital logic function. It uses LOW threshold voltage MOSFETs in the longest propagation path (critical path) to reduce the propagation delay of a logic function. Whereas it uses HIGH

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and MEDIUM threshold voltage MOSFET in rest of the circuit according to the needs in order to minimize the overall sub-threshold leakage current conduction and hence static power dissipation of the circuit.

This paper describes the low-power and high-speed design methodologies of a 1-bit Full-Adder, 8-bit-Ripple-Carry-Adder and finally a 4×4 Array Multiplier by MTCMOS using 2µm technology of TANNER EDA back-end tools. The power dissipation and propagation delay of the given logic circuits are verified at both Schematic level (using S_Edit) and Layout level (using L_Edit).

Implementation of 1-bit Full-Adder using MTCMOS logic

A 1-bit Full-Adder can be designed using 2 Ex-OR gates, 2 AND gates and 1 OR gate. Using Boolean function, the Sum and Carry outputs can be written as follows:

$$Sum = (A \oplus B \oplus C_{in})$$

$$Carry = AB + (A \oplus B).C_{in}$$

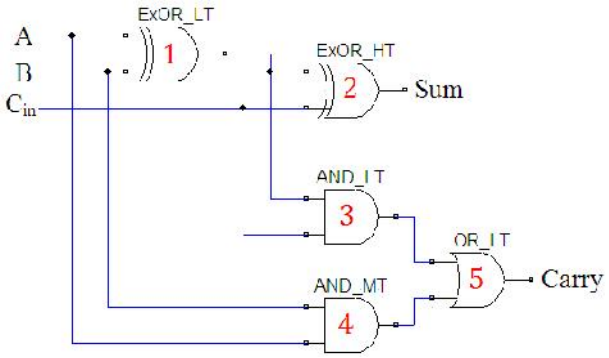


Fig1 Schematic of 1-bit Full-Adder

Table – 1: Threshold voltage variation of MOSFET in different logic gates

Gate No	Logic Gate	Threshold Voltage
1	ExOR	**LOW**
2	ExOR	**HIGH**
3	AND	**LOW**
4	AND	**MEDIUM**
5	OR	**LOW**

In Fig-1, the Carry path (Gate: 1-3-5) is the longest path (Critical Path), which has the largest propagation delay. So MT-CMOS technology uses LOW threshold voltage MOSFET to design the logic Gates - 1, 3 and 5 in order to reduce the Carry propagation delay of the circuit. But it unfortunately increases the overall power dissipation of the circuit as well. So to minimize the power dissipation, MT-CMOS technology uses very HIGH threshold voltage MOSFETs in Ex-OR gate (Gate-2) and MEDIUM threshold voltage MOSFETs in AND gate (Gate-4).

After performing the Simulation and Functional Verifications of the logic, the power dissipation and propagation delay of 1-bit Full-Adder is checked in from both S_Edit and L_Edit using TANNER EDA back-end tools.

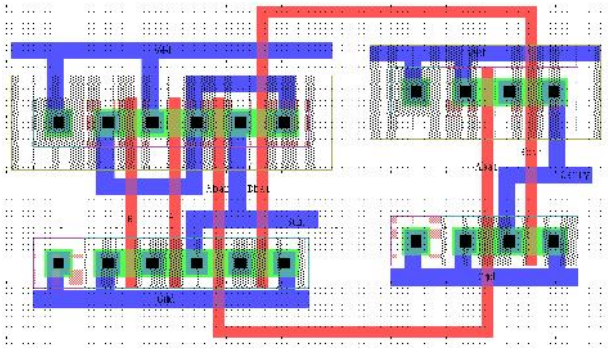


Fig2 Layout of 1-bit Full-Adder

The Table-2 gives the Experimental Results and compares the conventional and the proposed methodologies for 1-bit Full-Adder.

Table – 2: Comparison Table for **1-bit Full-Adder**

Parameters	Conventional Circuit	MTCMOS logic	% Reduction
Static Power Dissipation	1.25 µw	1.16 µw	7.2 %
Average Propagation Delay	7.625 ns	6.75 ns	11.4 %

Implementation of 8-bit Ripple-carry-Adder using MTCMOS logic

The 8-bit Ripple-carry-Adder is shown in Fig-3. It has total 17 inputs (A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3, A_4, B_4, A_5, B_5, A_6, B_6, A_7, B_7 and C_{in}) and 9 outputs (S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7 and C_{out}).

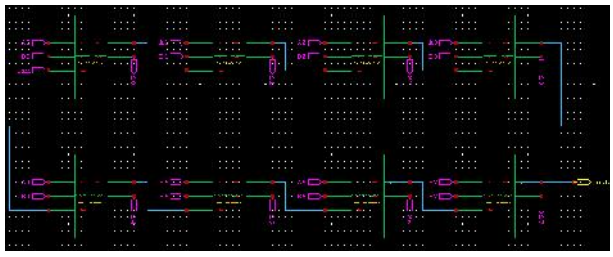


Fig-3 TOP Module of 8-bit Ripple-Carry-Adder

In the same way, the Carry path is still the longest propagation path in the 8-bit Ripple-Carry-Adder. The Carry outputs of every individual blocks are nothing but the Carry inputs of its subsequent block. MT-CMOS technology use LOW threshold MOSFET in the Carry propagation path of every individual blocks in order to speed-up the circuit operation. And it uses HIGH and MEDIUM threshold MOSFET in rest of the circuit to minimize the sub-threshold leakage current conduction and hence static power dissipation of the overall circuit. After performing the Simulation and Functional Verifications of the logic, the power dissipation and propagation delay of 8-bit

Ripple-Carry-Adder is checked using TANNER EDA back-end tools.

The Table-3 gives the Experimental Results and compares between the conventional and the proposed methodologies for 8-bit Ripple-Carry-Adder.

Table – 3: Comparison Table for **8-bit Ripple Carry Adder**

Parameters	Conventional Circuit	MTCMOS logic	% Reduction
Static Power Dissipation	10 µw	9.62 µw	3.8 %
Average Propagation Delay	7.75 ns	7.25 ns	6.4 %

So, the proposed methodologies reduces both power dissipation and propagation delay simultaneously in 8-bit-Ripple-Carry-Adder as well.

Implementation of 4×4 Array Multiplier using MTCMOS logic

Finally, the same logic is again applied in 4×4 Array Multiplier circuit**.**

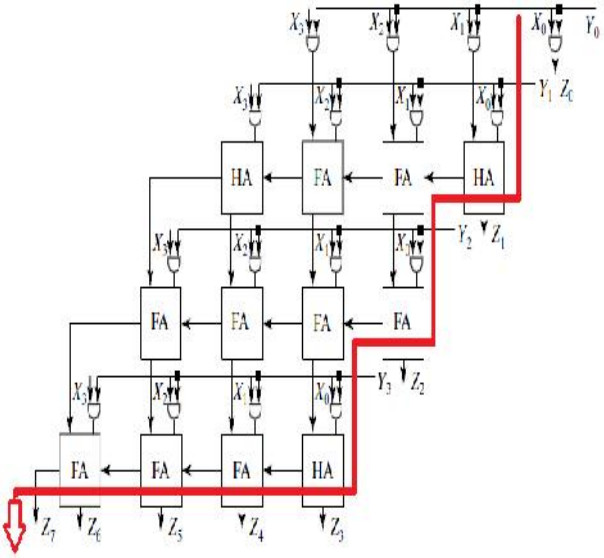


Fig-4 4×4 Array Multiplier logic diagram

In the Array Multiplier logic, the longest propagation path (Critical path) is marked in the Fig-4 (in Red Colour), which consists of 2 Half-Adders (HA) and 4 Full-Adders (FA).

In order to speed-up the above circuit, Carry propagation delay must be reduced in the critical path. This is done by using LOW threshold voltage MOSFETs of the Carry propagation paths in every Half-Adder (HA) and Full-Adder (FA) of the Critical path of this circuit.

But in order to minimize the power dissipation of the circuit, it uses the MEDIUM and HIGH threshold MOSFET in rest of the circuit where propagation delay is not that much important.

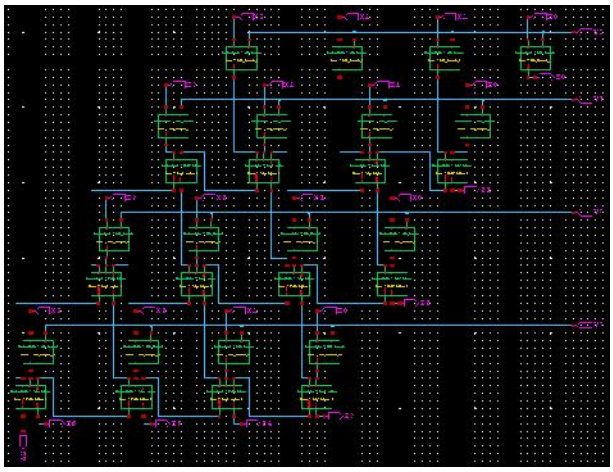


Fig-5 TOP Module of 4 × 4 Array Multiplier designed in S_Edit, TANNER EDA

After performing the Simulation and Functional Verifications of the logic, the power dissipation and propagation delay of 4×4 Array Multiplier is checked using TANNER EDA back-end tools.

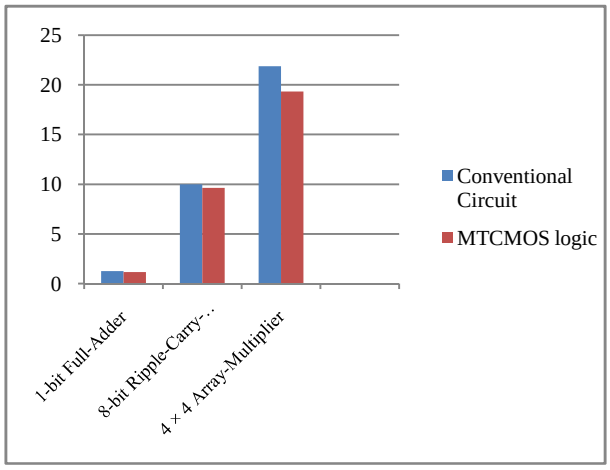
The following table gives the Experimental Results and compares between the conventional and the proposed methodologies for 4 × 4 Array Multiplier.

Table – 3: Comparison Table for **4 × 4 Array-Multiplier**

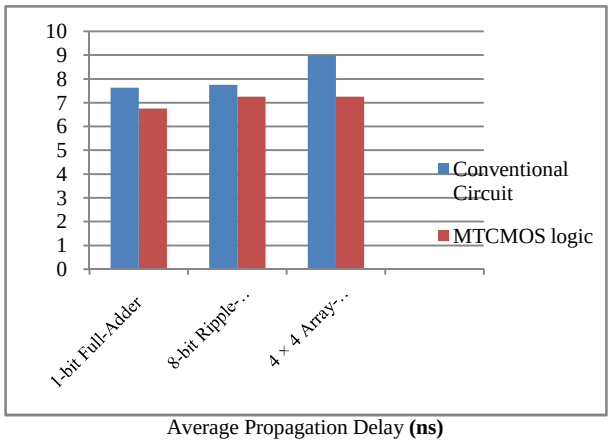
Parameters	Conventional Circuit	MTCMOS logic	% Reduction
Static Power Dissipation	21.87 µw	19.32 µw	11.65 %
Average Propagation	9.00 ns	7.25 ns	19.44 %

Analysis of Experimental Results

The proposed 1-bit Full-Adder reduces the Static power dissipation by 7.20% and the Average propagation delay by 11.40%. The proposed 8-bit Ripple-Carry-Adder reduces the Static power dissipation by 3.80% and the Average propagation delay by 6.40%.



Static Power Dissipation **(µw)**



Average Propagation Delay **(ns)**

The proposed 4 × 4 Array-Multiplier reduces theStatic power dissipation by 11.65% and the Average propagation delay by 19.44%.

CONCLUSION

This paper introduces the concept of low-power and high-speed digital logic design methodologies using Multi-threshold CMOS. It reduces the power dissipation in the shortest path and average propagation delay in the longest path (critical path).

Since this proposed technique does not include any additional components, so there is no area overhead. Hence the proposed methodology provides a better solution for the low power digital logic design.

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