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RESEARCH ARTICLE

POLYCRYSTALLINE PENTACENE BASED ORGANIC THIN FILM TRANSISTORS

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ABSTRACT

Metal-insulator-semiconductor organic thin film transistors (OTFTs) have been fabricated by the process of vacuum evaporation on glass substrates using pentacene ($C_{22}H_{14}$) as the active semiconductor and rare earth oxide viz. Dy_2O_3 as the gate insulator. The XRD of the pentacene thin films have been carried out and found to be polycrystalline in nature. The I-V characteristics of the OTFTs have been studied and analysed. The fabricated OTFTs are found to be p-type in nature and yielded highest field effect hole mobility of $9.2x10^{-3}$ $cm^2V^{-1}s^{-1}$. Our work demonstrates that the rare earth oxides are the promising gate dielectric materials for (OTFTs).

INTRODUCTION

Thin film active devices are structures consisting of one or more thin layers of metal, semiconductor and insulator. The thin film transistor (TFT) structure was first reported by Weimer in 1962 (Weimer, 1962). Basically a TFT is an insulated-gate field-effect transistor whose operation depends on the same basic principle as a metal oxide semiconductor field-effect transistor (MOSFET). The organic thin film transistors (OTFTs) are the transistors that use organic molecules as their active material.

Organic materials have been of interest for conductive and semiconductor applications for more than forty years. Since materials that allow bipolar conduction are not common, work on transistor structures has focused on field-effect devices, usually in the thin film form. However, field-effect mobilities of OTFTs have been disappointingly low, typically in the 10^{-5}-10^{-6} $cm^2V^{-1}s^{-1}$ range and too low for most applications (Lin *et al*., 1997). The playing field for OTFTs changed significantly when research focused on small molecule organic semiconductors, such as pentacene ($C_{22}H_{14}$). Recently a field effect mobility of 16 $cm^2V^{-1}s^{-1}$ has been reported for pentacene based devices (Mao *et al*., 2013)

Pentacene is a planar molecule composed of five benzene rings fused along their sides, as shown in Fig. 1. It has triclinic crystal structure with two molecules in each unit cell. Several other pentacene polytypes also exist. They differ only slightly in their molecular packing and exhibit similar single-particle energy band gaps ~1.9 – 2.2 eV (Northrup *et al*., 2003).

Organic thin film transistors are highly studied during last few years because of its variety of electronic applications, such as information display (Shin *et al.*, 2007), chemical sensors (Liao *et al.*, 2005, Halik *et al*., 2004), electronic paper (Han *e. al*. 2006) and microelectronics (Yi *et al*., 2005, Bartic *et al*., 2005).The potential advantages of organic TFTs are low cost, abundance of raw materials and above all the possibility of designing large area systems by using the simple techniques of vacuum evaporation and spin coating.

Experimental

In the present work OTFTs having channel length (L) 50 μm and channel width (W) 1mm, have been fabricated using pentacene as the active semiconducting material and Dysprosium Oxide (Dy_2O_3) as the gate insulator in the bottom-gate, bottom-contact architecture as shown in Fig. 2. For the source–drain and gate electrodes aluminium (99.9% pure) is evaporated at a vacuum better than $7x10^{-6}$ Torr. The amorphous rare earth oxide film of Dysprosium Oxide (Dy_2O_3) of 1200Å thickness (obtained from Loba Chemie in 99.99% pure form) is deposited to form the gate insulating layer. To form the active OTFT layer, pentacene of 99.97% purity (obtained from Aldrich Chem. Co.) is thermally evaporated at a vacuum better than 4 x 10^{-6} Torr with a deposition rate of 0.5 Å/s. The OTFTs so prepared are annealed at 100ºC for 5 hours in vacuum (6 x 10^{-6} Torr) and the electrical characteristics are then measured. In Fig. 3 the fabricated OTFTs are shown.

RESULTS AND DISCUSSION

In Fig. 4, the XRD pattern of the pentacene thin film deposited on glass substrate and without any annealing is shown. The observed diffraction peaks show that room temperature deposited thin film of pentacene is polycrystalline in nature. It is mainly due to the film deposition at ultrahigh vacuum conditions and at low deposition rate. In Fig. 5, the XRD pattern of the pentacene thin film deposited on glass substrate and annealed in vacuum at 100^{o}C is shown. The figure shows that after annealing the intensity of diffraction maxima increases significantly. This suggests that the annealing of the

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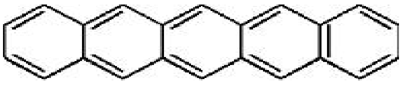

Figure 1 Structure of a pentacene molecule

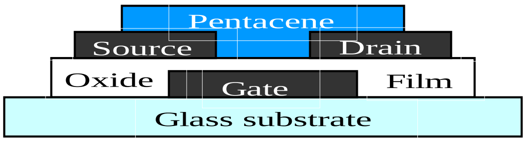

Figure 2 Structure of the OTFT

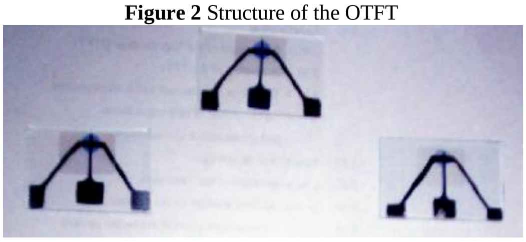

Figure 3 Fabricated OTFTs

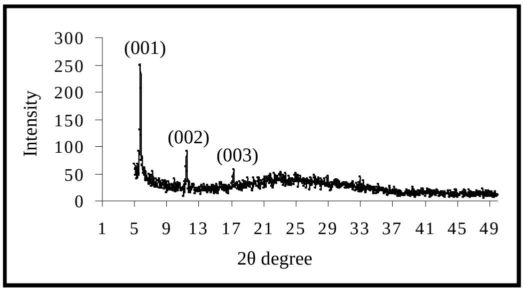

Figure 4 XRD pattern of the pentacene thin film (not annealed) deposited on glass substrate

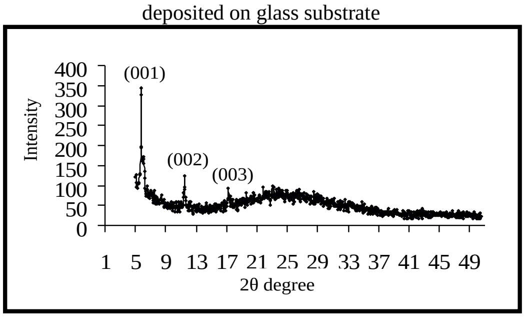

Figure 5 XRD pattern of the pentacene thin film (annealed in vacuum at 100°C) deposited on glass substrate

pentacene films in vacuum increases the size of the crystallites (or grains) along the *c*-axis and also the defects in the film, due to disoriented crystallites, are eliminated (Kang *et al.*, 2004).

The transistor characteristics curves, (plots of drain current I_D vs. source-drain voltage V_D at various gate voltages V_G), for the pentacene OTFTs (annealed in vacuum at 100°C) are shown in Fig. 6.

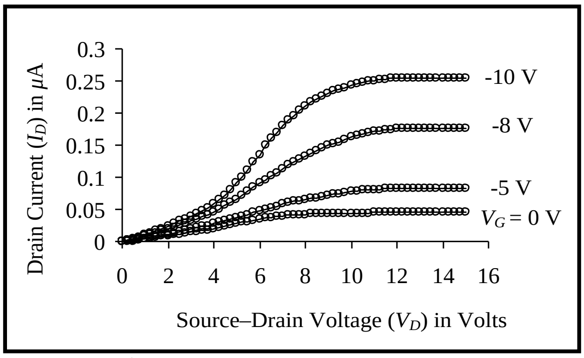

Figure 6 Plots of drain current I_D vs. source-drain voltage V_D at various gate voltages V_G

When the gate electrode is biased negatively with respect to the source electrode, the pentacene OTFTs operate in the accumulation mode and the accumulated charges are holes. At low V_D, I_D increases linearly with V_D (linear region) and is approximately given by (Dimitrakopoulos *et al.*, 1996).

$$I_D = \frac{WC_i}{L} « \left(V_G - V_T - \frac{V_D}{2} \right) V_D \quad (1)$$

Where L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, V_T is the threshold voltage and μ is the field effect mobility of the current carriers. The mobility (μ), in the linear region, can be calculated from the transconductance-

$$g_m = \left(\frac{\partial I_D}{\partial V_G} \right)_{V_D = const.} = \frac{WC_i}{L} « V_D \quad (2)$$

by plotting I_D vs. V_G at constant low V_D and equating to the value of the slope of this plot to the transconductance. The I_D vs. V_G plots of the OTFTs at low V_D = 4V are shown in Fig. 7.

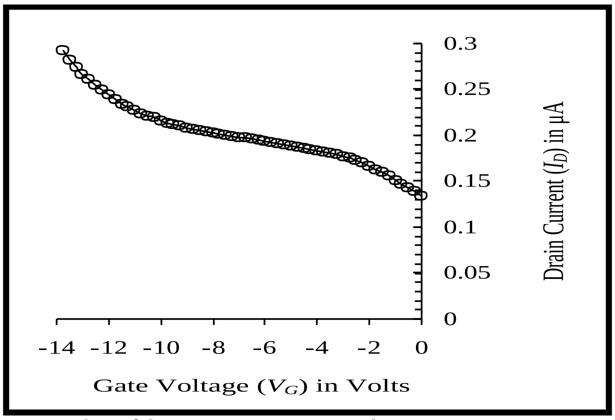

Figure 7 Plots of drain current I_D vs. gate voltage V_G at constant source-drain voltage V_D = 4 volts

Table 1 Transistor parameters of the pentacene based OTFTs

Transistor Parameters	Calculated values of the pentacene OTFTs	
	Annealed in vacuum at 100°C	Fresh (not annealed)
Capacitance per unit area (C_i)	1.69 x 10^{-8} F/cm^2	1.57 x 10^{-8} F/cm^2
Transconductance (g_m)	1.25 x 10^{-8} mho	1.04 x 10^{-9} mho
Field Effect Mobility (μ)	9.3 x 10^{-3} cm^{2}V^{-1}s^{-1}	7.6 x 10^{-4} cm^{2}V^{-1}s^{-1}

In Table 1 the various transistor parameters of the pentacene based OTFTs are listed. The mobility value indicates significantly improved performance for transistors with Rare Earth Oxide (REO) gate dielectric as compared to transistors with SiO_2 (Brown *et al.*, 1996, Horowitz *et al.*, 1992). Such an enhancement in the gate effect is due to higher dielectric constant (ε) of Dy_2O_3 film (ε =13.1 for Dy_2O_3) (Xue *et al.*, 2000) compared to SiO_2 (ε = 3.9), which leads to the increase in the gate capacitance C_i and results in much stronger gate effects for devices employing REOs as gate dielectric.

The field effect mobility for the freshly prepared and not-annealed OTFTs is found to be about one order less than those annealed in vacuum at 100°C. This indicates that annealing in vacuum decreases the trapping of charge carriers in grain boundaries of the polycrystalline semiconductor films. The OTFTs exposed to atmosphere for long time show a sharp degradation in their properties. This is due to the hygroscopic nature of the gate oxide material and therefore the encapsulated devices may show better result. The performance of the OTFTs is also affected by the roughness of the semiconductor-insulator interface and the thickness of the insulating film. The thinner oxides show smoother surface as well as higher capacitance than the thicker oxides (Lee *et al*., 2003). Therefore annealing of the oxide film prior to the semiconductor deposition can reduce the roughness of the oxide film surface which can lead to a better result of the prepared devices.

CONCLUSION

In conclusion we can say that pentacene based OTFTs can be fabricated using Dy_2O_3 as the gate insulator. The fabricated OTFTs have good performance comparable to those having SiO_2 as the gate insulator and have well defined I-V characteristics. Various parameters evaluated in this work give good understanding about the OTFT structure.

Acknowledgement

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