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Research Article

ALGORITHM BASED FPGA IMPLEMENTATION OF ADDRESS GENERATOR FOR WIMAX DEINTERLEAVER

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ABSTRACT

In brief, an optimized algorithm which is proposed early to over come the disadvantages of the Rom look-up table to implement the circuit for address generation for WiMAX Deinter leaver using Xilinx FPGA. According to IEEE 802.16E standard ,the implementation is very difficult, so algorithm is proposed which eliminates the floor function and thus it makes the FPGA implementation as less complexity, and now we optimized that proposed algorithm to make further less complexity by making high operating fvrequency and high latency. The implantation and resource utilization for quadrature phase-shift keying, 16-quadrature-amplitude modulation (QAM), and 64-QAM modulations along with all possible code rates makes this optimized algorithm be novel and high operating frequency when compared with early proposed algorithm. So this proposed optimized algorithm exhibits improvement in the resource utilization by optimizing the area

INTRODUCTION

Broadband wireless access (BWA) is present continuous challenging competitor to the conventional. Somany technologies[1]. Are evolved and IEEE has developed standards for mobile BWA (IEEE 802.16e) popularly referred to as mobile WiMAX [2]. The channel inter leaver employed in the WiMAX communication improve the errors origined.

In brief, an optimized low complexity, high speed, high operating frequency and latency for deinterleaver used in the WiMAX communication by deleting the required functions used. Few works are available in literature are available in physical implantation of deinterleaver used in WiMAX syatem. So many work to reduce the frequency access in deinterleaver using look-up table and also previously proposed algorithm on incoming data streams to reciver blocks shown in [3]. Khater *et al*.[4] described the VHDL language to describe the hardware implementation based on address generator according to IEEE 802.16e stsandard for interleaver with only ½ code rate. In [5], the authors show the Finite State Machine based address generator of the deinterleaver for all code rates and modulation schemes. [4] and [5] both are verified on Field programmable Gate Array logic base.

Hardware implementation of inter leaver functions is having complexity and also requires large number of resources[6].The look-up table ROM based method is not suitable because many reasons such as slow in operations and high consumption of resourses and etc. Comparing to this LUT based and also previously proposed algorithm will confirm the superiority of our optimized algorithm. In 16-QAM and 64-QAM, for the reason of 2-D translation in [6], a understandable and user friendly mathematical algorithm and equations is proposed. The all above is overcome by previously proposed algorithm, but our optimized proposed algorithm will stand firmly in front of it as it has high operating frequency and latency. And also our algorithm when realized by digital hardware results in low-complexity structure for generating address compared with previous technique and also its detiled structured presentation is shown in [6]. Here also authors consider the optimization techniques to make the compacted design between the quadrature phase-shift-key (QPSK), 16-QAM and 64-QAM.Here Spartan-3 FPGA is used to implement the above architecture in VHDL, or we can use Verilog. ModelSim is used as simulator to simulate their functional verification of proposed algorithm along with its hardware architecture results of both FPGA and proposed algorithm can be compare with the recent work are been made. Performance is improved by the embedded multipliers used in FPGA implementation due to reduced delay in between connections, resource utilization in efficient manner with low power consumption when compared to LUTY based and previpusly algorithm based tecniques.

In the next sections will briefly tell the following as follows: in section II the tecniques for interleaving communication for wimax, will be showed. In section III proposed algorithm. Transformation of our optimized algorithm into hardware structure is shown in section IV. Section V shows the

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simulation results. FPGA implementation is shown in section VI. Finally conclusion in section VII.

Techniques for Interleaving

The required blocks needed for wimax deinterleaver communication is showed in above fig.1. In that we can see the input data is sent by the source and before going to error correction that data should be randomized, before encoded by the error connection techniques. Reed-Solomon and convolution turbo code are the main error correction techniques used here. Then channel inter leaver allocate the free or specific channels to the input data streams. Then it going to mapped with the required channel and then inverse fourier transformation method is applied to that.

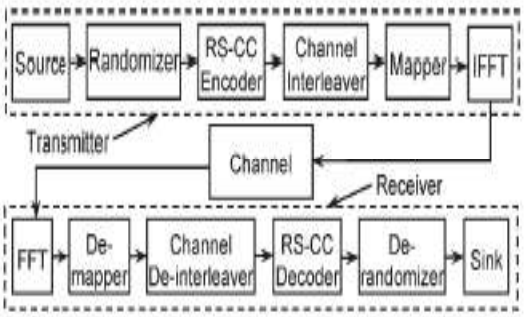

Figure 1 WiMAX transceiver blocks

Then it travels through the communication channel and freasch the reciver side and then it will be recived and fourier transformation is done to that and then again demapping and then this recived data will be once again realocation of channel by the de-interleaver then decoder and de-randomizer to check weather the data line recived and sent are same.

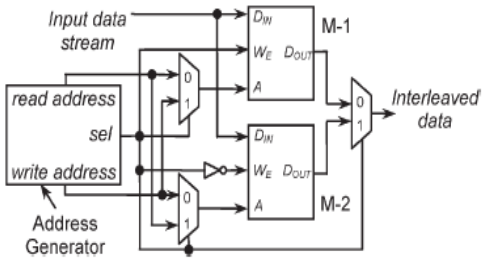

Figure 2 Interleaver/deinterleaver structure

The two dimensional interleaver/de-interleaver structure is showned in the above fig.2.In the select line is used to choose the read or write operation. When sel=1, write enabled signal is active and the recived address is written in the m-1 simultaneously, as the interleaved data is read from the M-2. After memory blocks are going by read/write operations then it automatically sel signal changes to write/read operation.

Ncbps, Different depths of interleaver blocks to incorporate various code rates and modulation schemes (see Table I) for IEEE 802.16e .The RS-CC encoder will permitted by the frecived data streams by cobining below [1] and [2].thus

$$m_k = \left(\frac{N_{cbps}}{d}\right) \cdot (k\%d) + \left\lfloor \frac{k}{d} \right\rfloor \qquad (1)$$

$$j_k = s \cdot \left\lfloor \frac{m_k}{s} \right\rfloor + \left(m_k - N_{cbps} - \left\lfloor \frac{d.m_k}{N_{cbps}} \right\rfloor\right)\%s \qquad (2)$$

Table 1 Inter leaver/Deinter leaver depth for modulation and full code types

Modulation Scheme	QPSK (s=1)		16-QAM (s=2)		64-QAM (s=3)		
Code Rate	½	¾	½	¾	½	⅔	¾
Interleaver Depth, N_{cbps} in bits	96	144	192	288	288	384	432
	192	288	384	576	576	-	-
	288	432	576	-	-	-	-
	384	576	-	-	-	-	-
	480	-	-	-	-	-	-
	576	-	-	-	-	-	-

Table 2 For starting 4- rows and 5-columns with 3 code-rate

N_{cbps}, code rate and modulation type	De-interleaver addresses				
N_{cbps} = 96-bits, ½ code rate, QPSK	0	16	32	48	64
	1	17	33	49	65
	2	18	34	50	66
	3	19	35	51	67
N_{cbps} = 192-bits, ½ code rate, 16-QAM	0	16	32	48	64
	17	1	49	33	81
	2	18	34	50	66
	19	3	51	35	83
N_{cbps} = 576-bits, ¾ code rate, 64-QAM	0	16	32	48	64
	17	33	1	65	81
	34	2	18	82	50
	3	19	35	51	67

Here d indicates the number of coloumn. Then the dent leaver reverse operations are also shown by two permutation ie..(3) and (4) which is shown in below

$$m_j = s \cdot \left\lfloor \frac{j}{s} \right\rfloor + \left(j + \left\lfloor \frac{a.j}{N_{cbps}} \right\rfloor\right)\%s \qquad (3)$$

$$k_j = d.m_j - (N_{cbps} - 1) \cdot \left\lfloor \frac{d.m_j}{N_{cbps}} \right\rfloor. \qquad (4)$$

Proposed Algorith

Here the previously proposed algorithm for address generator of wimax along with the mathermatical notations has been described. By using (3) and (4) a MATLAB program can be developed for all code rates and modulation schemes. Deinterleaver address for first 4-rows and 5-columns are shownede table.2.As d=16 is selected.

Table 3 Analyzing the correlation between addresses

Row no.(j)	Column no. (i) →	0	1	2	3	4
0	N_{cbps} = 96-bits, ½ code rate, QPSK	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.0+1=1	d.1+1=17	d.2+1=33	d.3+1=49	d.4+1=65
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67
0	N_{cbps} = 192-bits, ½ code rate, 16-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.0+1=1	d.3+1=49	d.2+1=33	d.5+1=81
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.1+3=19	d.0+3=3	d.3+3=51	d.2+3=35	d.5+3=83
0	N_{cbps} = 576-bits, ¾ code rate, 64-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.2+1=33	d.0+1=1	d.4+1=65	d.5+1=81
2		d.2+2=34	d.0+2=2	d.1+2=18	d.5+2=82	d.3+2=50
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67

A examination of the address in table.2 reveals the correlation between them follows the manner, as shown in table.3 the code notations used for QPSK QND QAM is shown below

A. QPSK

```
initializeNcbps and d
forj = 0 to d    1, j ++
fori = 0 to (Ncbps/d)    1, i++
kn= d   i + j
end for
end for
```

B. 16-QAM

```
initializeNcbps and d
forj = 0 to d    1, j ++
fori = 0 to (Ncbps/d)    1, i++
if (j mod 2 = 0)
kn= d   i + j
else
if (imod 2 = 0)
kn= d   (i + 1) + j
else
kn= d   (i    1) + j
end if
end if
end for
end for
```

C. 64-QAM

```
initializeNcbps and d
forj = 0 to d    1, j ++
fori = 0 to (Ncbps/d)    1, i++
if (j mod 3 = 0)
kn= d   i + j
elseif (j mod 3 = 1)
if (imod 3 = 2)
kn= d   (i    2) + j
else
kn= d   (i + 1) + j
end if
else
if (imod 3 = 0)
kn= d   (i + 2) + j
else
kn= d   (i    1)
end if
end if
end for
end for
```

Circuit Impementaion

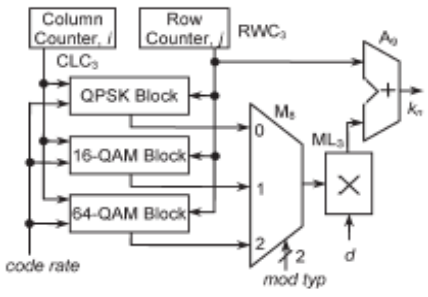

Fig.3 Complete Deinterleaver

The above all which we told in uor algorithm is converted into hardware implementation of complete deinterleaver address generator. In that we can see saperatecolumn counter and row counter to select row or column address to generate. Then in mod-2 it selects the outputs we want whether QPSK or QAM. Which is shown in above figure.

Simulation Result

The proposed above hardware of the address generator is converted into Verilog program using the Xilinx ISE. And corresponding Siulation results are obtained for all mod types and code types. The initial portion of fig.1 shows the last part of address for first row (j=1) and then the next part for second row (j=2).The simulation results are verified with the output from the MATLAB program described in section III.

Implementaion Result

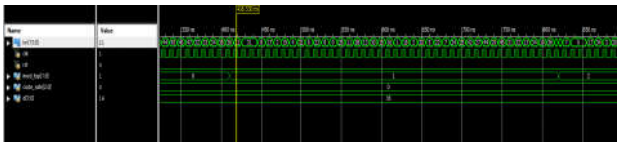

Figure-4 Simulation output

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	42	54576	0%
Number of Slice LUTs	44	27288	0%
Number of fully used LUT-FF pairs	42	44	95%
Number of bonded IOBs	18	218	8%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Figure-5 synthesis report

FPGA Parameters	Performance of proposed technique	Performance of LUT based technique	% Reduction / improvement in resource utilization	Remarks
Slices	3.49 %	17.66 %	-80.24	Significant reduction
Flip Flops	0.50 %	0.78 %	-35.90	Reduction
4 input LUTs	3.35 %	17.15 %	-80.47	Significant reduction
Operating frequency	121.82 MHz	62.51 MHz	48.69	Significant improvement

Figure-6 Previous algorithm list

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 4.569ns (Maximum Frequency: 218.861MHz)
   Minimum input arrival time before clock: 5.673ns
   Maximum output required time after clock: 8.621ns
   Maximum combinational path delay: 9.582ns
```

Figure-7 present optimized algoritham operating frequency

In above figure-4 represents the synthesis report for our hardware implementation of our address generator. In figure-5 represents the resource utilization and also it tabulated the operating frequency of the previously pro [osedalgorithm. In the figure -6 we can see the operating frequency of our optimized proposed algorithm and also we can note the improvement of the operating frequency in our optimized algorithm.

CONCLUSION

This brief has proposed a optimized algorithm along with its mathematical formulation. Comparision of our optimized proposed algorithm with a previously proposed algorithm

method and also recent work show significant improvement on resource utilization, operating frequency and latency.

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