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RESEARCH ARTICLE

APPLICATIONS OF TOFFOLI GATE FOR DESIGNING THE CLASSICAL GATES USING QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

Quantum dot Cellular Automata (QCA) is an emerging technology for development of logic circuits based on nanotechnology, and is one of the alternative for designing high performance computing over existing CMOS-VLSI technology. QCA does not use voltage level for logic representation rather it represents binary state by polarization of electrons in the QCA Cell. Conventional logic circuits are irreversible in nature and always lead to energy dissipation. Thus extensive research is going on to design the circuits which does not dissipation the energy and hence will not loose the information. In this paper we have designed the QCA based toffoli gate and then implemented the basic logic gates with it. The circuits were successfully simulated and verified by QCA Designer tool.

INTRODUCTION

The Complementary Metal Oxide Semiconductor (CMOS) provides micro scale computing, with high density and low power very large-scale integration (VLSI) system. However such system faces many problems like high leakage current, high lithography cost, and limitation of speed in GHz range. As a result there is a need to find out an alternative of CMOS technology. One of strong alternative technology is a Quantum-dot Cellular Automata. QCA utilize the quantum effects that come with a small size and its basic element is quantum dot cell where the logic state is encoded as the position of electrons with in a cell rather than the voltage levels. This novel idea was first proposed by researcher Dr. Craig Lent (Lent *et al,* 1993; Lent and Tougaw, 1997) at university of Notre Dame. The QCA cells have the features of very low nanometer scale, much smaller than the smallest transistor, and gets better as the dimensions are reduced. In the QCA technology, binary information is stored in the charge configuration of single cells and transferred via Coulomb coupling between neighbouring cells (Tougaw & Lent, 1994)

Low power design is one of the primary goal of Very Large-Scale Integration (VLSI). Landauer in 1961 (Landauer, 1961) proved that traditional binary irreversible gates lead to power dissipation in a circuit regardless of implementation. Each bit of information that is lost, generates KT *ln*(2) Joules of heat energy, where K is Boltzmann's constant (≈1.380658 × 10^{23} J/K) and T the absolute temperature (Kelvins) at which computation is performed. For room temperature T the amount of dissipating heat is small (i.e. 2.9 × 10^{21} J), but not negligible (Maslov, 2003; Dueck & Maslov, 2003; Maslov & Dueck, 2003) Bennett in 1973 showed that for power not to be dissipated in an arbitrary circuit, it is necessary that this circuit be built from reversible gates. The importance of Bennett's theorem lies in the technological necessity that every future technology will have to use reversible gates in order to reduce power loss (Bashaga, 2007; Bennett, 1973; Thapliyal, 2006). Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors (Lukac & Pivtoraiko, 2002; Toffoli, 1980). Hence Reversible logic design is preferred for the design of combinational as well as sequential circuit.

Traditional logic functions (such as AND, OR) are not reversible, because more than one input state is mapped to a common output state. In such condition, given the output state, it is not possible to determine initial input states. Inverter (INV) is a simple example of a reversible logic gate. The most studied reversible logic gates are the Toffoli (Toffoli, 1980), Feynman (Feynman, 1985) and the Fredkin gate (Parhami, 2006).

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Besides Toffoli and Fredkin gates, various other reversible gates have also been proposed (Khan, 2002; Peres, 1985; Islam, *et al*, 2002; Biswas, *et al*, 2008; Haghparast & Navi, 2008; Bhagyalakshmi & Venkatesha, 2010; Nayeem, Jamal, & babu, 2009; Bhagyalakshmi & Venkatesha, 2011). Reversible logic is emerging as a promising computing paradigm with applications in ultra-low power nano computing and emerging nanotechnologies such as quantum computing, quantum dot cellular automata (QCA), optical computing, DNA computing etc.

QCA Basic

The basic element of the Quantum dot cellular automata is the QCA cell which consists of four quantum dots positioned at four corners of cell and two mobile electrons confined within the cell (Frost, *et al*, 2002). In QCA, logic state is determined by the polarization of electrons rather than voltage level as in CMOS technology. The two stable polarization of electrons are P= -1.00 and P= +1.00 of a QCA cell represents binary logic '1' and logic '0' respectively, as shown in (Figure 1).

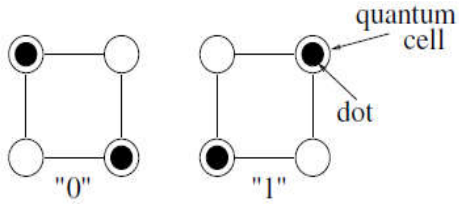


Figure 1 QCA cell polarizations and representations of binary 0 and binary 1

It is possible to implement all combinational and sequential logic functions by properly arranging cells so that the polarization of one cell sets the polarization of a nearby cell. According to previous studies, several logic gates and computing devices (Tougaw & Lent, 1994) are implemented with QCA. The basic elements of QCA are:

Majority Gate

The majority logic gate is shown in (Figure 2a). It consists of three inputs labeled as a, b, c and single output. The centre cell is referred as driver cell and it switches to major polarization and maintains a constant output. The logic equation of the majority gate can be realized as:

$$M(a,b,c)=ab+bc+ac$$

The majority gate can be programmed to either function as an AND or an OR gate by fixing the polarization of any one of the input cells as P= -1 or P= +1. As shown in (Figure 2b and 2c).

$$M(a,b,-1)=a.b$$
$$M(a,b,1)=a.+b$$

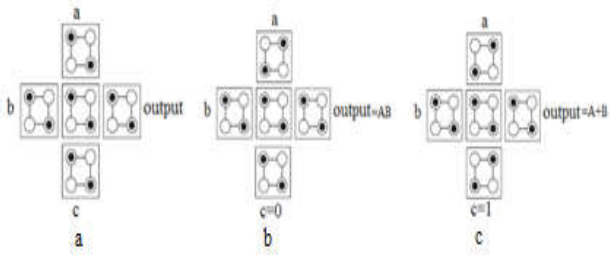


Figure 2 (a) Majority Gate. (b) Majority AND gate. (c) Majority OR gate.

Inverter

The QCA cells can be used to form the primitive logic gates. The simplest structure is the inverter shown (Figure 3)

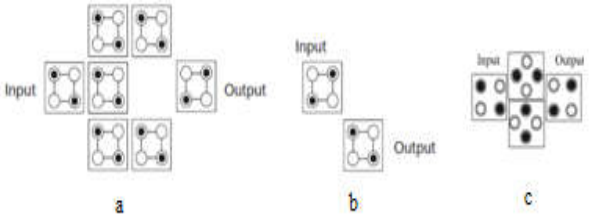


Figure 3 (a) Seven cell inverter (b) two cell inverter (c) four cell inverter.

There are three main types of inverters used in the QCA technology. (Figure 3a) shows the seven cell inverter which operates properly in almost all the circuits because of strong polarization. The input polarization split into two polarizations and at the end the two wires join and make the reverse polarization. The second type of inverter is a two cell inverter which is designed with the two cells which are vertically displaced as shown in (Figure 3b). The other type of inverter is a four cell inverter shown in (Figure 3c). The two vertical cells are rotated while as the two horizontal cells in which one represents the input and the other represents the output are normal cells.

QCA Wire

There are two types of wires in QCA, 90^0 QCA wire and 45^0 wire as shown in (Figure 4).

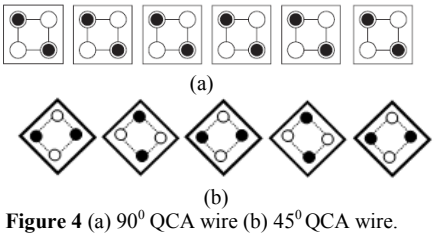


Figure 4 (a) 90^0 QCA wire (b) 45^0 QCA wire.

The 90^0 QCA wire is simply an array of cells arranged in a cascaded fashion. The polarization of each cell is affected by the electrostatic force due to coulombic repulsion generated by the neighboring cells. Thus information propagates down from one cell to another through the QCA wire. The 45^0 wire comprise of rotated cells and the signal alternates between the input value and its logic complement as it traverses the chain towards the output.

QCA Wire Crossing

One of the unique property of the QCA is the capability to create the different signal wire crossings. There are two types of wire crossings available in QCA: Coplanar crossing and multi layer crossing. A coplanar crossing (Tougaw & Lent, 1994) is implemented by one layer only. A coplanar crossing uses both regular and rotated cells as shown in (Figure 5a). These cells do not interact with each other if properly aligned. On the other hand the multi layer crossing is implemented using more than one layer. Multi layer crossings are expected to achieve more reliable results (Gin, Tougaw, & Williams, (1999), but they are difficult to fabricate. The multi layer

crossing is shown in (Figure 5b).

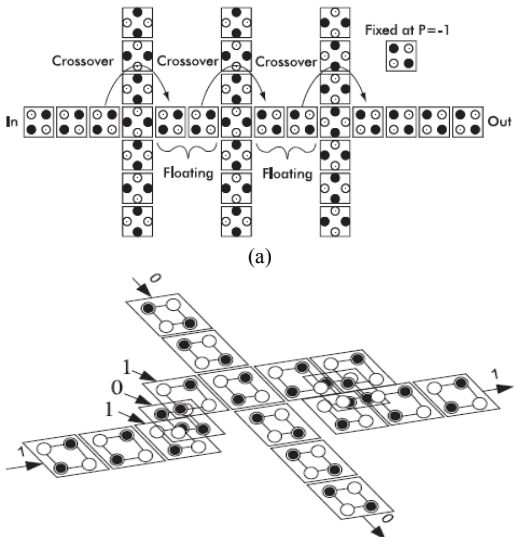
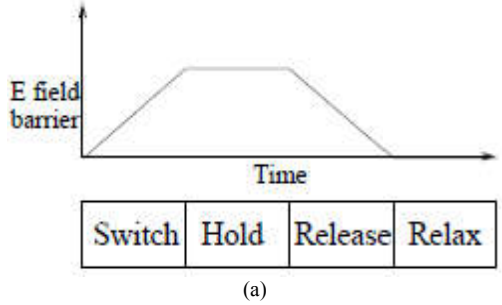


Figure 5 (a) Coplanar wire crossing (b) Multi layer wire crossing.

QCA Clock

Timing in QCA is accomplished by clocking in four distinct and periodic phases (Hennessy, & Lent, (2001). and is needed for both combinational and sequential circuits. Clocking provides not only control of information flow but also true power gain in QCA (Lent, & Isaksen, 2003). A QCA cell has four clock zones and each clock zone has four phases Switch, Hold, Release and Relax as shown in (Figure 6). During the switch phase, QCA cells begin to become unpolarized and their inter-dot potential barriers are low. The barriers are then raised during this phase and the QCA cells become polarized according to the state of their driver (*i.e.* their input cell).

It is in this clock phase that the actual computation (or switching) occurs. By the end of this clock phase, barriers are high enough to suppress any electron tunneling and cell states are fixed. During the hold phase, barriers are held high so the outputs of the sub array can be used as inputs to the next stage. In the release phase, barriers are lowered and cells are allowed to relax to an unpolarized state. Finally, during the fourth clock phase, the relax phase, cell barriers remain lowered and cells remain in an unpolarized state. In a QCA circuits, information is transferred and processed in a pipelined fashion (Antonelli, *et al*, 2004) and allows multi-bit information transfer for QCA through signal latching. All cells within the same zone are allowed to switch simultaneously, while cells in different zones are isolated.



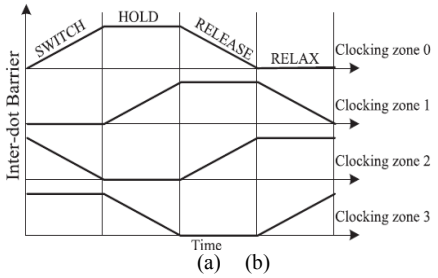


Figure 6 (a) 4 phase clocking. (b) Switching in a binary wire

Toffoli Gate

Toffoli gate is also known as controlled-controlled NOT gate (CCNOT). Toffoli gate is universal logic gate and any logic function can be constructed using toffoli gates only. It is a 3 x 3 gate means it has three inputs and three outputs. The input vector is $I(A,B,C)$ and the output vector is $O(P,Q,R)$. The outputs are defined as: $P=A$, $Q=B$ and $R=AB\oplus C$ respectively. The schematics and the MV representation of the toffoli gate is shown in (Figure 7a & 7b)

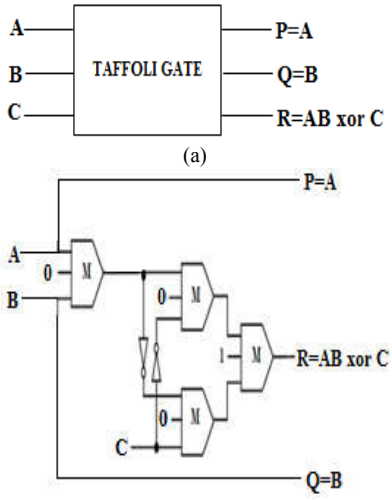


Figure 7 (a) Block Diagram of toffoli gate. (b) MV representation of Toffoli gate.

The truth table of the toffoli gate is given in table1.

Table 1 Truth table of Toffoli gate.

Inputs			Outputs		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

From the table1 it is clear that the first two outputs (P and Q) are equal to inputs while the third output(R) is inverted when the first two inputs are equal to 1. The toffoli gate is the universal gate the basic logic gates can be easily constructed with it. For any boolean function $f(x1,x2,x3....xn)$ there is a circuit consisting of toffoli gates which takes $(x1,x2,x3,....xn)$ as inputs and provides the $(y1,y2,y3,....yn)$ as outputs. Any boolean function can be implemented using OR, AND and NOT gates, which may be combined to form any boolean equation.

Mathematically the toffoli gate can be represented as:

$$Toffoli(a,b,c) = \begin{cases} (a,b,c') & when\ a=b=1 \\ (a,b,c) & otherwise \end{cases} \quad (1)$$

The QCA implementation and the simulation results are shown in (Figure 8 & 9)

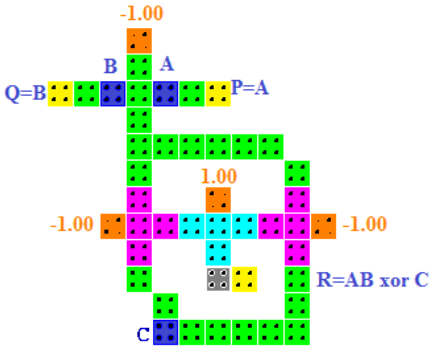


Figure 8 QCA implementation of Toffoli gate.

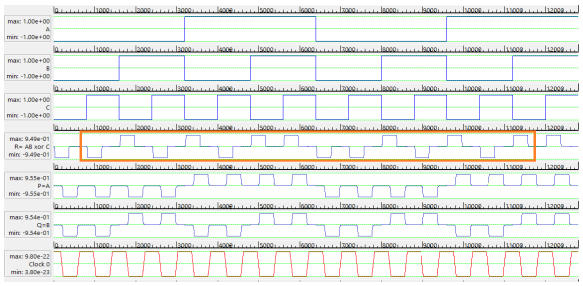


Figure 9 Simulation Result of Toffoli gate

The toffoli gate is designed with four majority gates. One majority gate provides the AND function and the other three perform the XOR operation. The outputs P and Q are garbage outputs and are not required in the computations. The comparison of the various QCA based toffoli gate and the proposed one is given in the table2.

Table 2 Comparison of various toffoli gates

Circuit	No. of Layers	Cell count	Cell Area (μm^2)	Total Area(μm^2)	Latency(in clock cycles)
Toffoli gate(Shafi, 2015)	1	57	0.0184	0.0700	3
Toffoli gate[Lombardi, 2008]	3	169	0.0547	-	16
Toffoli gate(Bahar,2013)	1	48	0.0155	0.0498	4
Toffoli gate(Bahar,2013)	1	75	0.0243	0.0952	4
Toffoli gate(Cvetkovska, 2013)	1	101	0.0327	0.0829	5
Proposed Toffoli gate	1	45	0.0145	0.0427	4

As evident from the table 2 that the proposed QCA toffoli gate is efficient in terms of cell count, cell area, total area, latency and complexity as compared to the previous designs available in the open literature. As the toffoli gate as the universal gate and thereby selecting the proper inputs the basic logic gates can be designed by using the above generalized equation as:

$$NOT(A)=Taffoli(A,1,1) \quad (2)$$

$$AND(A,B)=Taffoli(A,B,0) \quad (3)$$

$$OR(A,B)=Taffoli(\overline{A},\overline{B},1) \quad (4)$$

$$NAND(A,B)=Taffoli(A,B,1) \quad (5)$$

$$NOR(A,B)=Taffoli(\overline{A},\overline{B},0) \quad (6)$$

$$EXOR(A,C)=Taffoli(A,1,C) \quad (7)$$

$$EXNOR(A,C)=Taffoli(A,1,\overline{C}) \quad (8)$$

The QCA implementation of the various logic gates designed with the toffoli gate is shown in the (Figure 10 a-g).

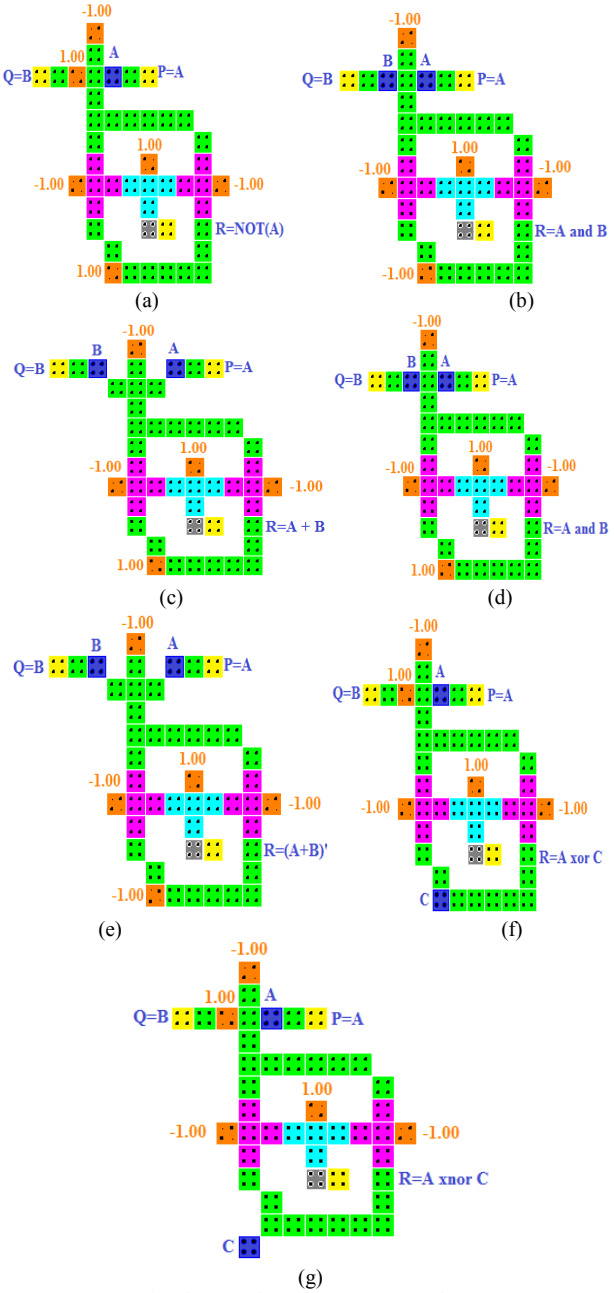
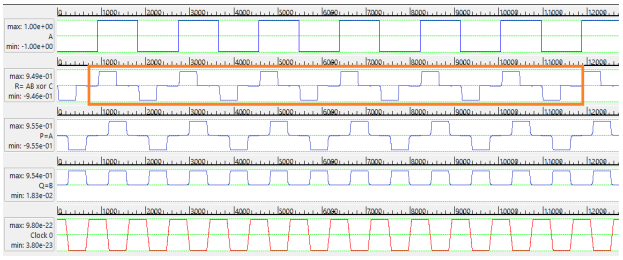


Figure 10 QCA implementation of (a) NOT gate (b) AND gate (c) OR gate (d) NAND gate (e) NOR gate (f) EX-OR gate (g) EX-NOR gate.

The simulation results of the various toffoli gate QCA based logic gates are given in (Figure 11 a-g).



(a)

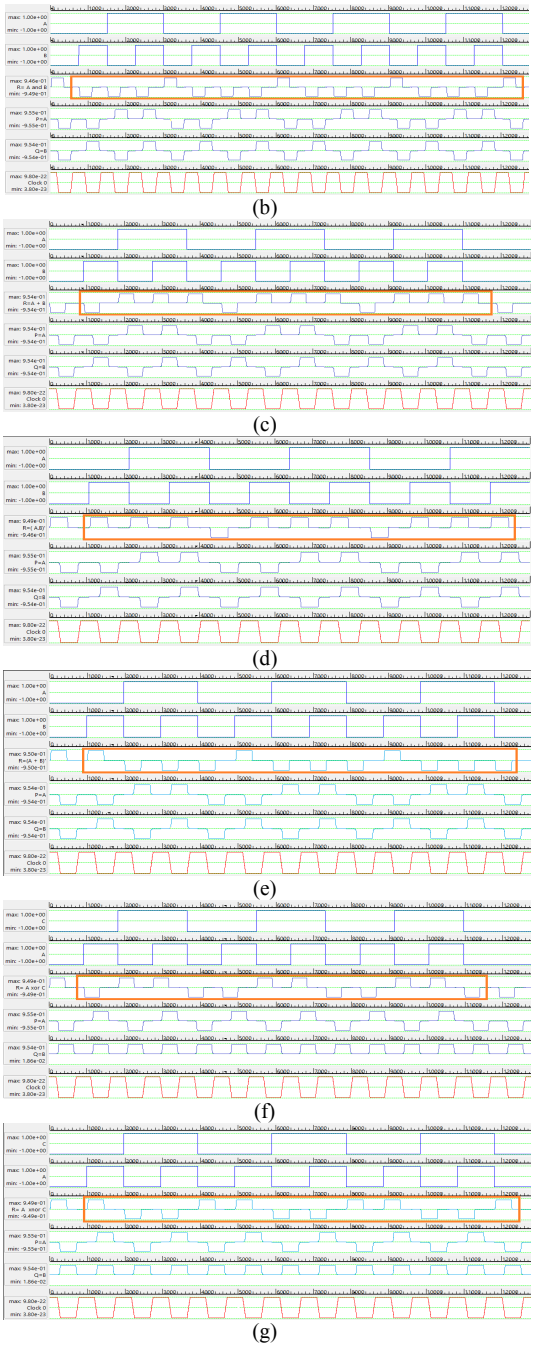


Figure 11 Simulation results of (a) NOT gate (b) AND gate (c) OR gate (d) NAND gate (e) NOR gate (f) EX-OR gate (g) EX-NOR gate .

The simulations were carried out using the QCA Designer tool using the bistable approximation under the following specified parameters.

- Cell size=18nm,
- Cell spacing 2nm
- Number of Samples=12800
- Radius of Effect =65.000000nm
- Convergence Tolerance=0.001000
- Relative Permittivity =12.900000
- Clock High =9.800000e-022
- Clock Low =3.800000e-023
- Clock Shift =0.000000e+000
- Clock Amplitude Factor =2.000000
- Layer Separation =11.500000.

CONCLUSION

In this paper, toffoli gate was implemented using quantum dot cellular automata. As the toffoli gate is the universal gate, the proposed QCA implementation of toffoli gate can be extended to design the classical logic gates. The proposed QCA structures are efficient in term of cell count, cell area, latency and complexity can be used in the design and development of combinational and sequential circuits that would prove to be beneficial in respect of power saving, reduction of garbage outputs and less amount of delay. Besides, being reversible will enjoy low energy dissipation, simple testability and increased fault detection features.

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