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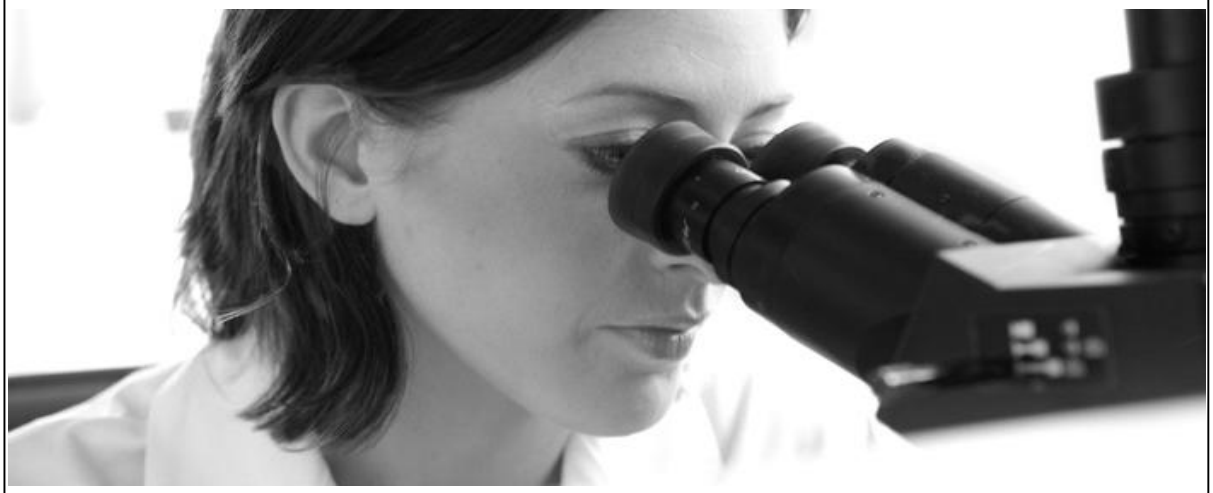

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RESEARCH ARTICLE

A LOW POWER DESIGN OF IP-SRAM ARCHITECTURE AT DEEP SUBMICRON CMOS TECHNOLOGY

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ABSTRACT

The increasing demand for high density VLSI circuits the leakage current on the oxide thickness is becoming a key challenge in deep-sub-micron CMOS technology. The leakage power becomes a key for a low power design due to its increasing proportion in chip's total power consumption in deep submicron technologies. Leakage power dissipation is playing a pivotal role in the total power decadence as threshold voltage becomes low as it is motivated by emerging battery-operated application on one hand and declining technology of deep sub micron on the other hand. Due to the difference between power, area and performance, various attempts have been done. This work is also based to minimize the power profligation of the VLSI circuits with the execution up to the acceptable level. Here we suggested Novel SRAM architecture called IP-SRAM with distinct write sub-cell and read sub-cell. In this paper we designed the total 8 bit SRAM architecture with newly suggested techniques and contrast this one with conventional SRAM architecture and we observed that the total power consumption is minimized. Here we used 180nm technology to design the total architecture. These results are contrasted this with deep submicron technologies.

INTRODUCTION

SRAMs strongly affect the over- all power, performance, stability and area requirements. They must be specially designed for target applications in order to manage constrained tradeoffs, because in the modern Digital Systems-on-Chip (SoCs) the Static Ram (SRAM) is a critical component [1]. The fast growth in semiconductor technology has led to the reduction of feature sizes of transistors using deep submicron (DSM) process. The undesirable consequences regarding power consumption arise as MOS transistors enter deep submicron sizes. Currently, dynamic or switching power component dominated the total power dissipated by an IC. In order to decrease dynamic power due to the square law dependency of digital circuit active power on the supply voltage, voltage scaling is the most effective method. As a result, in order to maintain performance we have to reduce the threshold voltage. Lower threshold voltage results in an exponential increase in the sub-threshold leakage current. On the other hand shorter channel lengths result in increased sub-threshold leakage current through an off transistor as technology scales down. Therefore, in DSM process static or leakage power becomes a considerable measure of the total power dissipation. Because of these reasons, static power consumption, i.e. leakage power dissipation, has become a significant part of total power consumption for current and future silicon technologies.

In this paper we present some VLSI techniques to reduce leakage power. Each and every technique provides a systematic way to reduce leakage power. Here in this paper we designed SRAM cell [2]. with low power techniques with 180nm technology

Conventional 6-T Sram Cell

Static RAM(SRAM) is a kind of semiconductor memory that uses bistable-latching circuitry (Flip-flop) to store each bit. SRAM is a type of volatile memory in the conventional sense that data is eventually lost when the memory is not powered. They are nearly universally found on the same die with microcontrollers and microprocessors, because they are fast, resilient, and easily manufactured in standard logic processes. Due to their greater speed SRAM based Cache memories and System-on-chips are commonly used.

There are several design challenges for nanometer SRAM design due to device scaling. Low power SRAM design is critical since it takes a large amount of total power and die area in high performance processors. A SRAM cell must meet the fullfillments for the operation in submicron/nano ranges. The scaling of CMOS technology [3] has remarkable affects on SRAM cell random fluctuation of electrical characteristics and substantial leakage current.

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The figure 1 shows the schematic of SRAM cell. As from the figure it contains two pull up PMOS and two NMOS pull down transistors as two cross coupled inverters and two NMOS access transistors to access the SRAM cell during the Write and Read operations [4]. Both the bit lines (BL and BLB) are used in order to transfer the data during the read and write operations in a differential means. The data signal and its inverse is provided to BL and BLB respectively in order to have better noise margin. The data stored is represented as two stable states, at storing points VR and VL, and denoted as 0 and 1.

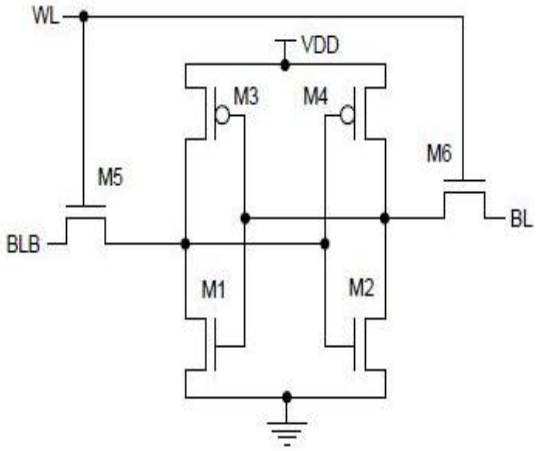

Figure 1 Conventional 6-T SRAM

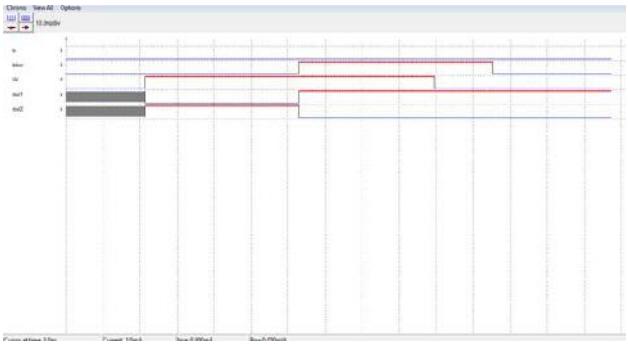

Figure 2 Simulation results for conventional SRAM cell

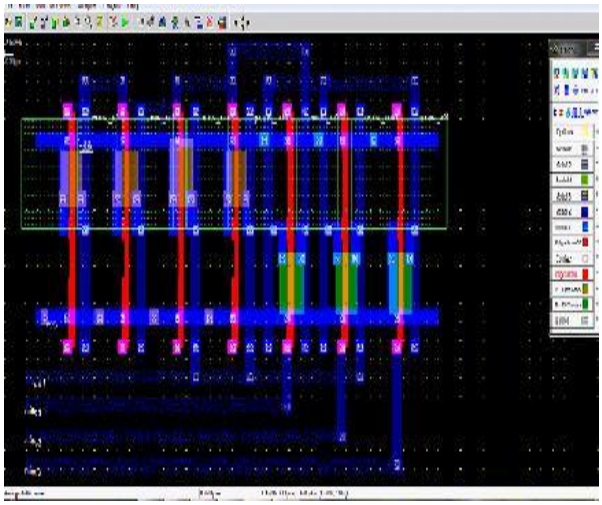

Figure 3 Layout for conventional SRAM cell

Lfs - Sram Cell

In power gated leakage feedback with stack (LFS), we are combining two techniques that is ultra low power technique or Stack approach and leakage feedback approach due to less transistor than sleepy-stack in which we replaces each transistor in base case into three transistors, and here we are combining these two techniques.

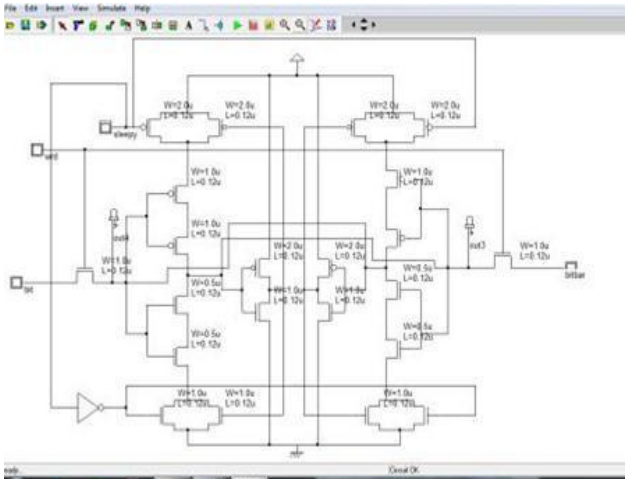

Figure 4 Schematic for LFS-SRAM cell

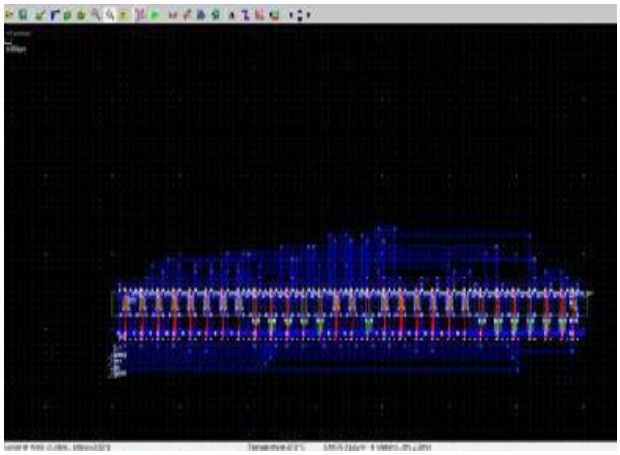

Figure 5 Layout for LFS-SRAM cell

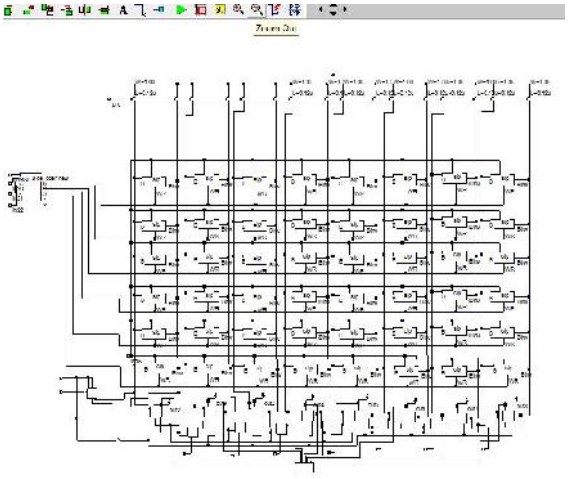

Figure 6 Schematic for IP-SRAM Architecture

IP-Sram Cell

In the novel power gated Improved P3 (IP) SRAM Cell, the union of two separate sub-cells (write and read) structure is proposed with a pMOS gated ground and drowsy stratagem to reduce the active and standby power without losing the cells performance. The data write and memory storage is done at

upper sub-cell while lower sub-cell is used for data read operation only. In active mode of operation, the cell supplied with VDD [6]. In data write mode, the data read sub-cell is completely obscured from data write sub- cell across BL‟s and vice-versa, which further improves the cells stability.

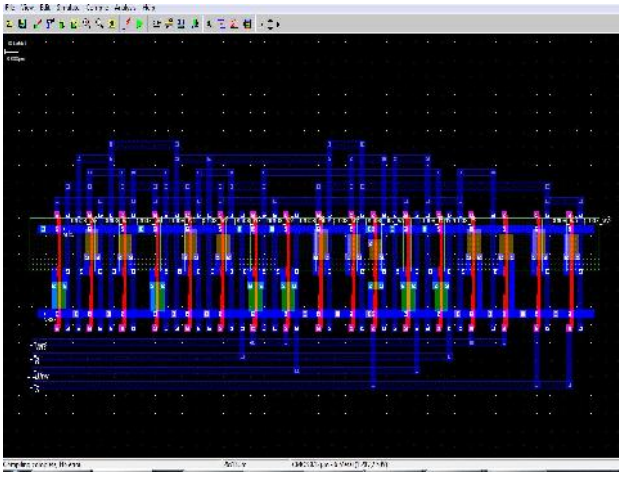

Figure 7 Simulation results for IP-SRAM cell

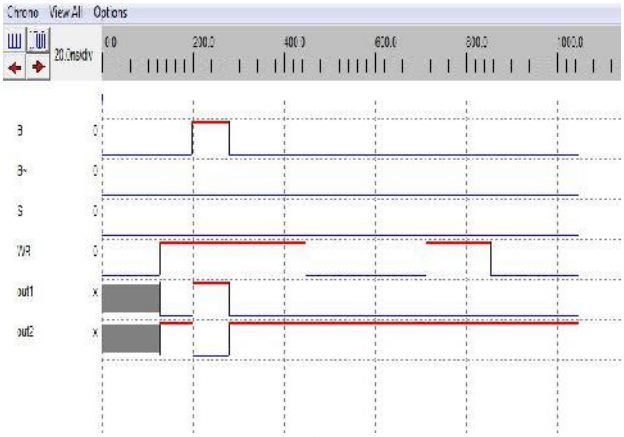

Figure 8 Layout for IP-SRAM cell

CONCLUSIONS

In this paper we designed a reduced power consumption SRAM architecture with IP-SRAM technique. we have separate read and write operations in this IP-SRAM technique and to reduce power consumption we are placing one PMOS device in between pull down network and ground. Here 180nm technology is used to design the total SRAM architecture and we observed that the IP-SRAM architecture have less power consumption as compared to basic SRAM architecture. Hence it is concluded that the suggested SRAM Architecture is used for low power designs and these designed techniques are used for high performance and low power applications.

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