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RESEARCH ARTICLE

IMPLEMENTATION AND EVOLUATION OF ADIBATIC LOGIC

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ABSTRACT

Low power has emerged as a principle theme in today electronic industry. Energy efficiency is one of the most important features of modern electronic systems designed for high speed and portable applications. The power consumption of the electronic devices can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. This paper presents an energy efficient technique for sequential and combinational circuits that uses adiabatic logic. The proposed technique has less power dissipation when compared to the conventional CMOS design style. This paper evaluates the sequential and combinational in different adiabatic logic styles and their results were to be compared with the conventional CMOS design.

INTRODUCTION

Design

Adiabatic design is developed to overcome the power dissipation problems in CMOS design which is the most concern aspect in present day VLSI technology. Adiabatic logic is implemented by placing two AC sources in which one source is out of phase with the other and two sources are connected to ground. The recovery process can be done in such a way that the charge is stored in capacitor while charging phase and while discharging the energy is recycled by the second AC source and again used in the circuit. The adiabatic design can be shown as follows

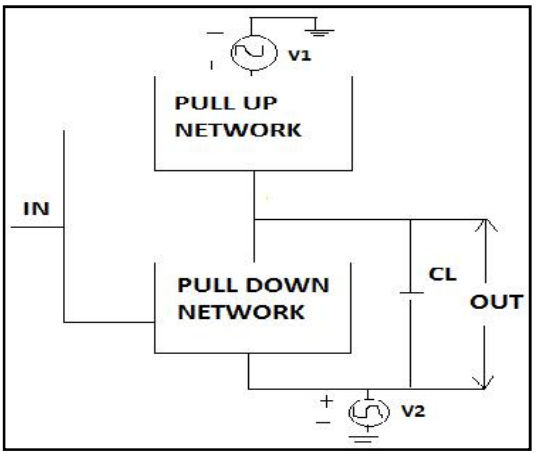

Fig Adiabatic Charging And Discharging

The basic CMOS inverter and adiabatic inverter circuits can be shown as follows

Cmos Inverter

The basic CMOS inverter circuit is shown in figure

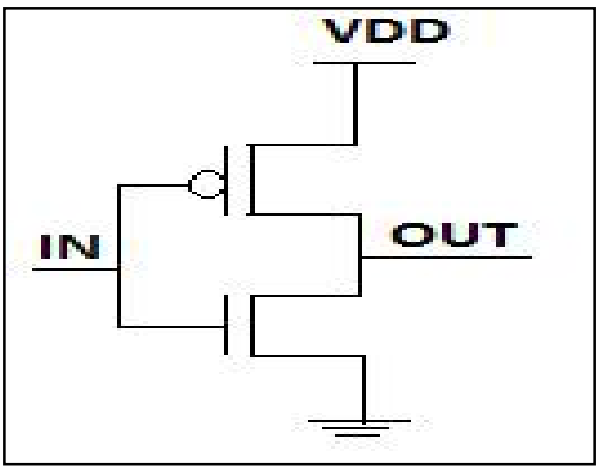

Fig CMOS Inverter

The operation of the circuit can be evaluated in two stages of charging phase and discharging phase. During the charging phase, the input to the circuit is logic LOW. During this phase, the pMOS transistor conducts and NMOS transistor goes in to OFF state which charges the output value to power supply results in logic HIGH output. The equivalent circuit consists of a resistor in series with the output load capacitance which

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shows a charging path from power supply to output terminal. Here the resistor acts as pMOS ON resistor.

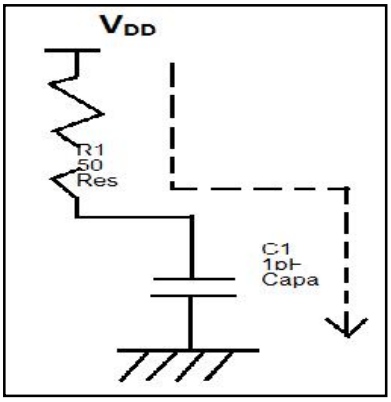

Fig Charging Phase

During the discharging phase, the input to the circuit is logic HIGH. During this phase, the nMOS transistor conducts and pMOS transistor goes into OFF state which results in a discharging path from output terminal to ground. The value that is stored at the output during the charging phase discharges towards the ground results in logic LOW output. The equivalent circuit consists of a resistor in series with output terminal to ground. Here the resistor acts as nMOS ON resistor.

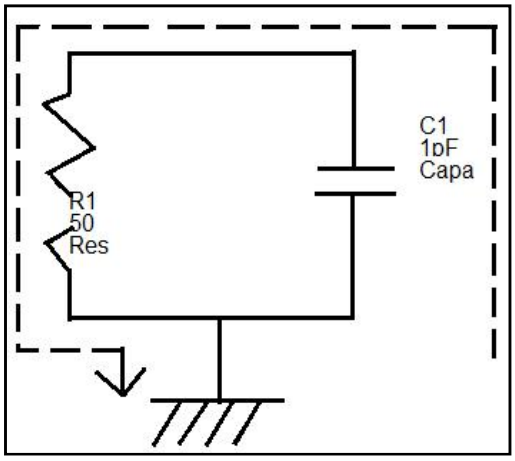

Fig Discharging Phase

From the operation of the CMOS design it is evident that during the charging process, the output load capacitor is charged to $Q = C_L V_{dd}$ and the energy stored at the output is $(½)C_L V_{dd}^2$. During the discharging phase, the amount of energy dissipated is also $(½)C_L V_{dd}^2$. So the total amount of energy dissipated during the charging and discharging phases is

$$E_{dissipated} = C_L V_{dd}^2$$

Adiabatic Inverter

The word ADIABATIC is derived from the Greek word “adiabatos”, which means there is no exchange of energy with the environment and hence no energy loss in the form of heat dissipation. Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as “energy recovery” or “charge recovery” logic. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases.

The adiabatic logic uses AC power supply instead of constant DC supply, this is one of the main reasons in the reduction of power dissipation. The adiabatic logic can be explained with the help of basic inverter circuit.

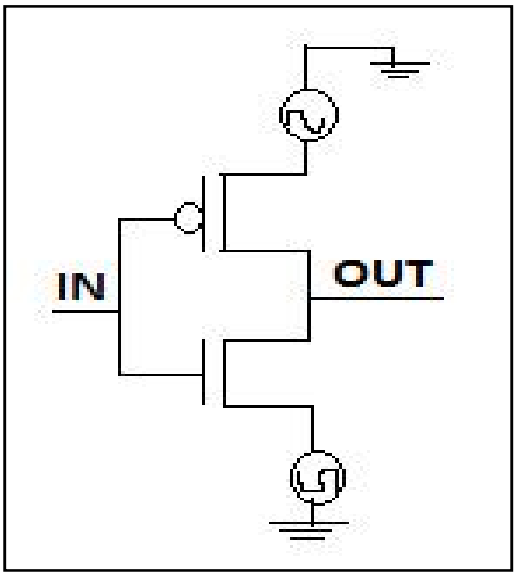

Fig Adiabatic Inverter

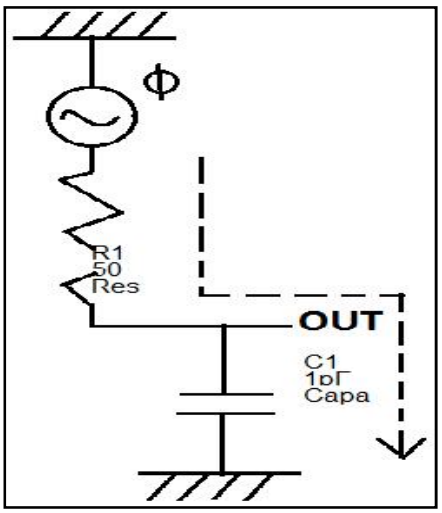

Fig Charging Phase of Adiabatic Inverter

The adiabatic inverter circuit can be constructed using CMOS inverter with two AC power supplies

instead of DC supply. The power supply's are arranged in such a way that one of the clock is in phase while the other is out of phase with the first one. The operation of the adiabatic inverter can be explained in two stages. During the charging phase, the pMOS transistor conducts and nMOS transistor goes into OFF state which charges the output load capacitor towards the power supply results in logic HIGH output.

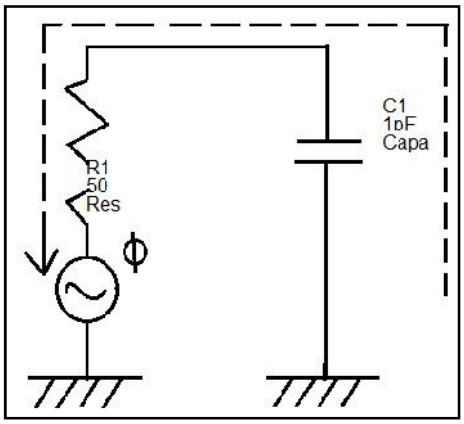

Fig Equivalent Circuit For Charge Recovery Process in Adiabatic Inverter

During discharging phase, the nMOS transistor conducts and pMOS transistor goes into OFF state. Instead of discharging the stored value at the output towards ground, the energy is recycled back to the power supply. Its equivalent circuit consists of a resistor in series with output load capacitance and power supply.

The charging process and the charge recovery process are efficient only when the charging voltage is varying one. Lower the rate of charging, lesser the power drawn from the supply voltage.

Adiabatic Techniques

Adiabatic logic has a different logic style which helps in the reduction of the power dissipation of the circuit. Some of the important adiabatic techniques are

Ecrl

Efficient charge recovery logic (ECRL) consists of two cross couple pMOS transistors in the pull up section where as the pull down section is constructed with a tree of nMOS transistors. Its structure is similar to Cascode Voltage Switch Logic (CVSL) with differential signalling. The logic function in the functional block can be realized with only nMOS transistors in the pull down section. The basic inverter in ECRL logic can be constructed as

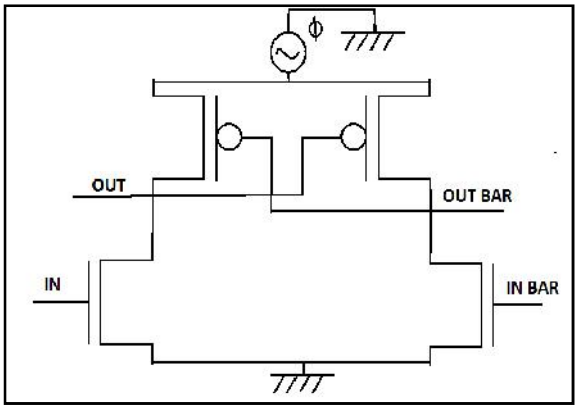

Fig ECRL Inverter

Pfal

The Positive Feedback Adiabatic Logic (PFAL) is a partial energy recovery circuit. It is also known as PAL-2N (Pass transistor Adiabatic Logic). The core of PFAL logic is a latch made up of two pMOS and two nMOS transistors that avoid logic level degradation on the output nodes. Using PFAL, the basic inverter can be constructed as

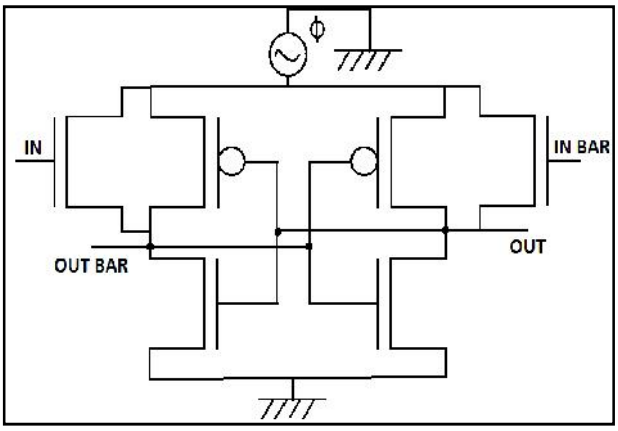

Fig PFAL Inverter

The logic function in the functional block can be realized with only nMOS transistors connected parallel to the pMOS transistors. The primary advantage of PFAL over ECRL is that the functional blocks are in parallel with the PMOSFETs forming transmission gate. It also has the advantage of implementing both the true function and its complimentary function.

PASCL

The Two Phase Adiabatic Static Clocked Logic (2PASCL) uses two phase clocking split level sinusoidal power supply's which has symmetrical and unsymmetrical power clocks where one clock is in phase while the other is out of phase. The circuit has two diodes in its construction where one diode is placed between the output node and power clock,

and another diode connected between one of the terminals of nMOS and power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. The circuit operation is divided into two phases "hold phase" and "evaluation phase". During the evaluation phase, the power clock swings up and power source swings down. During the hold phase, the power source swings up and power clock swings down.

Using 2PASCL the basic inverter can be constructed as

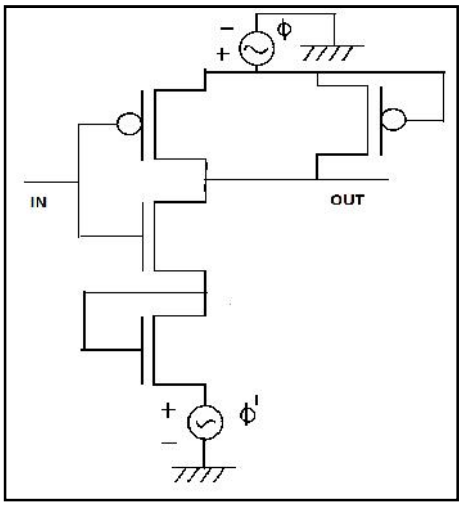

Fig 2PASCL Inverter

CONCLUSION

This paper proposes energy efficient adiabatic logic for digital circuits. The results were simulated using micro-wind tool and comparison has been done for different parameters of combinational & sequential logics in different adiabatic styles and CMOS design. The results show that the proposed adiabatic logic has less power dissipation compared to conventional CMOS design and it also uses less power supply.

These advantages made this logic more convenient for energy efficient digital applications.

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