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Research Article

ANALYSIS OF MODIFIED REED SOLOMON ERROR CORRECTING CODES

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ABSTRACT

In a Satellite or Tele Communication channel there is a high probability of corruption of data. So it is very much important to establish a reliable channel for communication. In order to overcome this problem, many error correcting techniques were introduced over time. Among all Reed-Solomon is the most popular technique. Reed – Solomon codes are an important sub – class of non-binary BCH codes. These are cyclic codes and are very effectively used for the detection and correction of burst errors. Galois field arithmetic is used for encoding and decoding of Reed – Solomon codes. Galois field multipliers are used for encoding the information block. At the decoder, the syndrome of the received codeword is calculated using the generator polynomial to detect errors. Then to correct these errors, an error locator polynomial is calculated. From the error locator polynomial, the location of the error and its magnitude is obtained. Consequently a correct codeword is obtained. RS Codes are implemented using VHDL and the functional working of the modified architecture has been tested using modelsim.

INTRODUCTION

All the advancements in the field of communication are to be achieved through reliability and efficiency. In most cases reliability is given the priority over efficiency though at certain cases one is compromised for the other. Reliability of communication has an impact even in our day to day life. For example message received on our mobile phone may become unreadable if some error occurs during the transmission, or a scratch in our DVD may make it unreadable. There are wide ranges of concern in the field of digital communication [1].

Generally communication is understood as transmission and reception of data from one place to other at some distance. If we change the reference it can also include transmission and reception of data at the same place but at a different point of time, which means storage and retrieval of data. Hence storage is also a part of communication. In any system application we come across errors either in communication or in storage. Errors in transmission are mainly because of noise, electromagnetic interferences, cross talk, bandwidth limitation, etc. In case of storage, errors may occur because of increase in magnetic flux as in case of magnetic disc or it can be spurious change of bits because of electromagnetic interferences as in case of DRAM. Hence dealing with these errors when they occur is the matter of concern.

The first step is to detect the error. And after the error gets detected there are two alternate approaches to proceed [2]. Forward error correction (FEC) approach, error is both detected and corrected at the receiver end. To enable the receiver to detect and correct the data, some redundant information is sent with the actual information by the transmitter. After being introduced to both the approaches, one should choose whether which approach is to be used. Automatic repeat request is easier but if the error occurs much frequently, then retransmission at that frequency will particularly reduce the effective rate of data transmission. However, in some cases retransmission may not be feasible to us. In those cases, Forward Error correction would be more suitable. As Forward Error Correction involves additional information during transmission along with the actual data. It also reduces the effective data rate which is independent of rate of error. Hence, if error occurs less frequently then Automatic request approach is followed keeping in mind that retransmission is feasible.

Out of the various FEC's, Reed Solomon code is one. These are block error correcting codes with wide range of applications in the field of digital communications. These codes are used to correct errors in devices such as CD's, DVDs etc.., wireless communications, many digital subscriber lines such as ADSL, HDSL etc… They describe a systematic way of building codes that can detect and correct multiple errors. In a

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block code we have k individual information bits, r individual parity bits and a total of n (=k+r) bits. However, reed Solomon codes is organized in group of bits. These groups of bits are referred to as symbols. So we can say, this code has n number of symbols. Each symbol comprises of m number of bits, where maximum value of n is 2^m -1 [3] and [4].

The Reed-Solomon code is well understood, relatively easy to implement provides a good tolerance to error bursts and is compatible with binary transmission systems.

RS codes belong to the family known as block codes. RS codes are non-binary systematic cyclic linear block codes. Non-binary codes work with symbols that consist of several bits. A common symbol size for non-binary codes is 8 bits, or a byte. The encoder applies a reversible mathematical function to the message symbols in order to generate the redundancy, or parity, symbols. The codeword is then formed by appending the parity symbols to the message symbols. The implementation of a code is simplified if it is systematic. A code is considered to be cyclic if a circular shift of any valid codeword also produces another valid codeword. Cyclic codes are popular because of the existence of efficient decoding techniques for them. Finally, a code is linear if the addition of any two valid code words also results in another valid codeword [5].

RS codes are generally represented as an RS (n, k), with m-bit symbols, where block Length is n, no. of original Message symbols are k, number of Parity Digits are n - k = 2t and minimum Distance is d which is equal to 2t + 1.Non-binary codes such as RS are good at correcting burst errors because the correction of these codes is done on the symbol level. By working with symbols in the decoding process, these codes can correct a symbol with a burst of eight errors just as easily as they can correct a symbol with a single bit error [6] and [7]. Whereas Codes Such as Viterbi or Turbo Codes are good at correcting random errors but they fail in correcting burst errors which commonly happen in most of the communication medium. Because of this unique feature RS codes are preferred in most of the ASDL Networks, Cellular and mobile phones and High definition televisions. The communication system model is shown in figure 1.

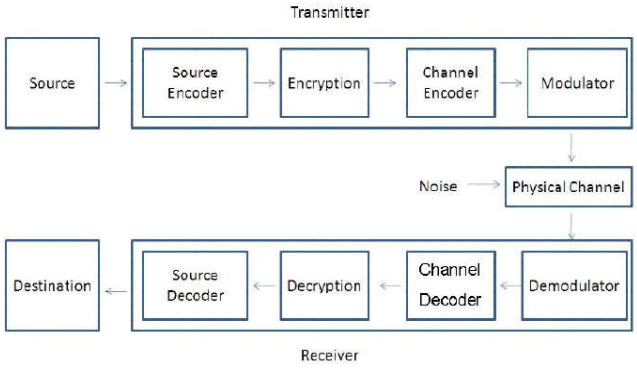

Figure 1 Communication System

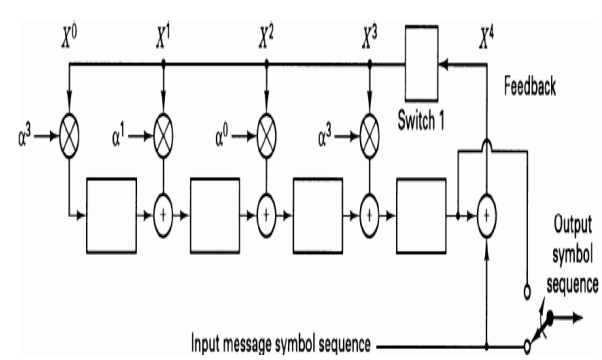

Figure 2 RS Encoding block diagram using LFSR

RS Encoding and decoding

RS codes are systematic, so for encoding, the information symbols in the codeword are placed as the higher power coefficients. This requires that information symbols must be shifted from power level of n-1 down to n-k and the remaining positions from power n-k-1 to 0 be filled with zeros. Therefore any RS encoder design should effectively perform the following two operations, namely division and shifting. Both operations can be easily implemented using Linear-Feedback Shift Registers as shown in figure 2.

The parity symbols are computed by performing a polynomial division using GF algebra. The steps involved in this computation are as follows:

- Multiply the message symbols by Xn-k. This shifts the message symbols to the left to make space for the n-k parity symbols.
- Divide the message polynomial by the code generator polynomial using GF algebra.
- The parity symbols are the remainder of this division. These steps are accomplished in hardware using a shift register with feedback [8], [9] and [10].

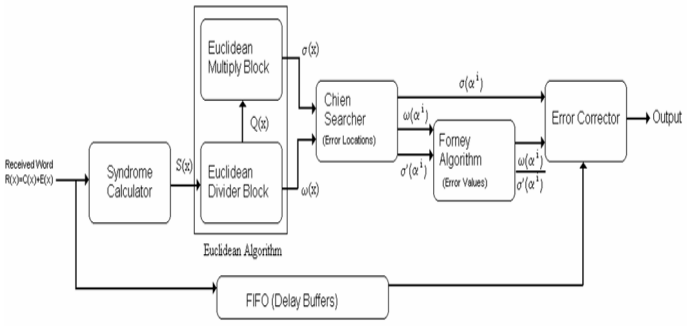

Figure 3 Flow Diagram of RS Decoder

A typical decoder follows the following stages in the decoding cycle, namely syndrome calculation, determine error-location polynomial, solving the error locator polynomial - Chien search, calculating the error magnitude and error correction as shown in figure 3.

Modified Architecture of Rs Codes

Most of the existing architectures of the Reed Solomon coding systems are limited by value of m and t, in order to serve the real time situation of variable block length the existing architecture is modified as shown in figures 4 and 5.

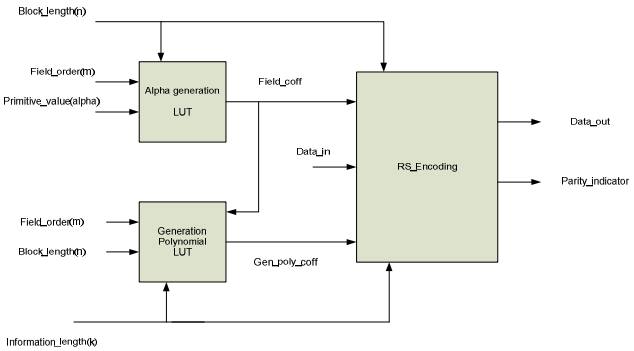

Figure 4 Modified Architecture of RS Encoder

As the block length Varies, the value of m and also varies accordingly. The Galois Field values and Generator polynomial and primitive polynomial also varies in accordance with value of m. In order to generate field coefficients and generator polynomial coefficients a Look up Table (LUT) based approach is followed.

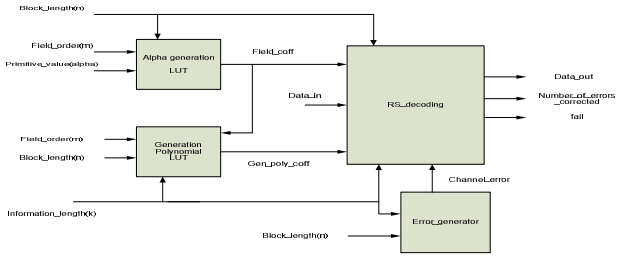

Figure 5 Modified Architecture of RS Decoder

SIMULATION RESULTS

Reed Solomon Encoder and Decoder has been designed in C and then VHDL using Xilinx ISE 12.3 and Simulation level debugging is performed using Modelsim 6.6e [11].

Figure 6 shows the test case the
Input Data: M=4; N=15;
K=9; T =3;
The following output will be generated for corrupted data in information bits. Error Introduced in 13th location

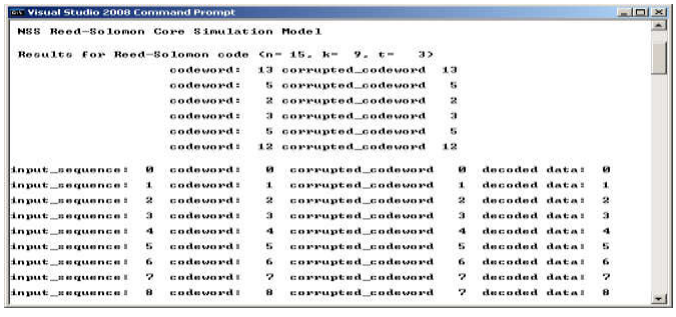

Figure 6 Test Case Result of Reed Solomon Codes

Figure 7 shows the results with the ramp input to system.
A triangular Input is given to Reed-Solomon Error Correcting System, below results show us the error corrected triangular waveform (with additional parity) at the decoder output as shown in figure 8.

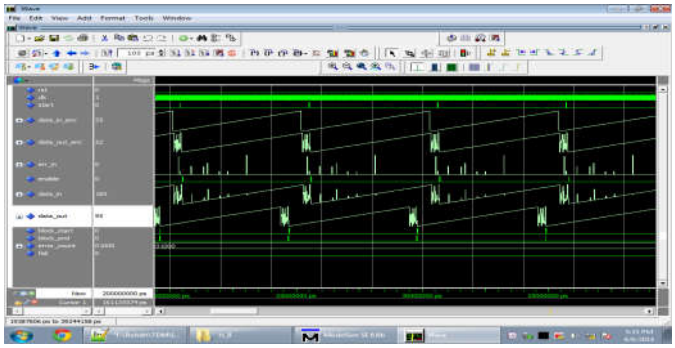

Figure 7 Simulation Results of Reed Solomon Codes

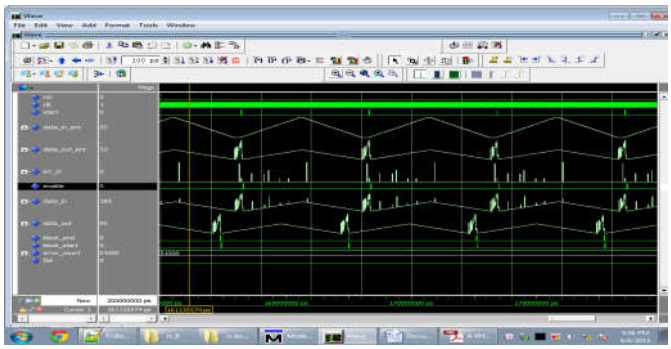

Figure 8 Results of Reed Solomon Codes with triangular waveform

Figure 7 shows the data_in_enc is input to the encoder (ramp waveform) and data_out_enc can be observed as a ramp with some redundant data so called parity symbols added at the end of encoding err_in shows the error introducing assuming channel does some damage to the information data_in is the input to the decoding system with errors and on signal data_out can be observed data with no errors. Block_start and block_end bifurcates block data error_count tells us the number of errors corrected in the previous block fail indicates that the system is failed to retrieve data in the previous block.

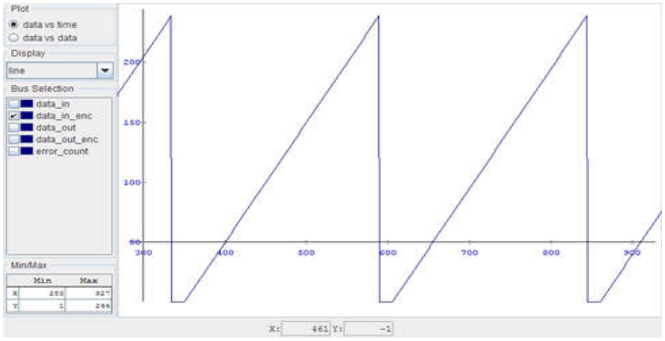

Figure 9 Ramp input to the RS system

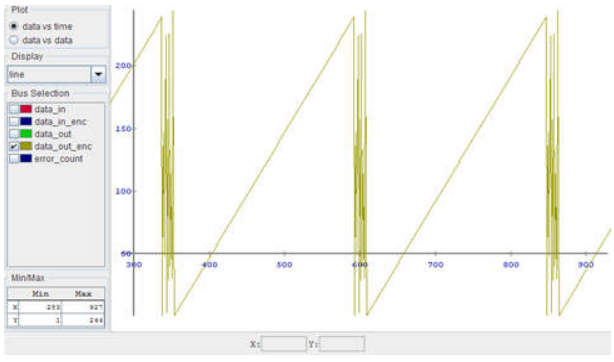

Figure 10 Encoded output of the RS system

The figures 9, 10, 11, 12 and 13 show the Hardware proven System with applied ramp waveform at the Input of encoder and Introducing Noise bits at the end of Encoder output and feeding that noise added Signal to decoder Input and observing original ramp input at the decoder output.

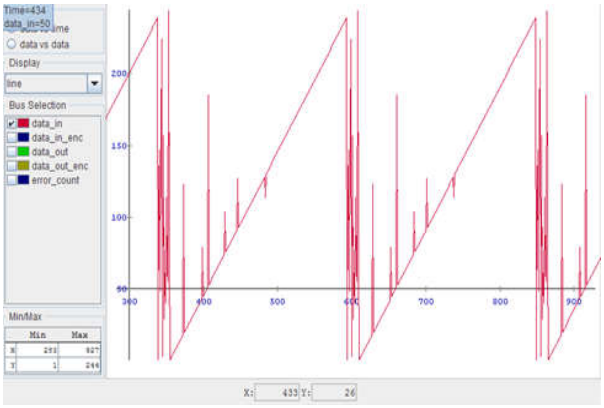

Figure 11 Input to the decoder of RS system with errors

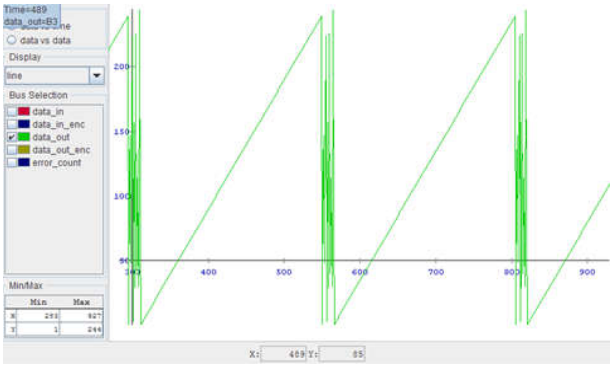

Figure 12 Decoded output of the RS system

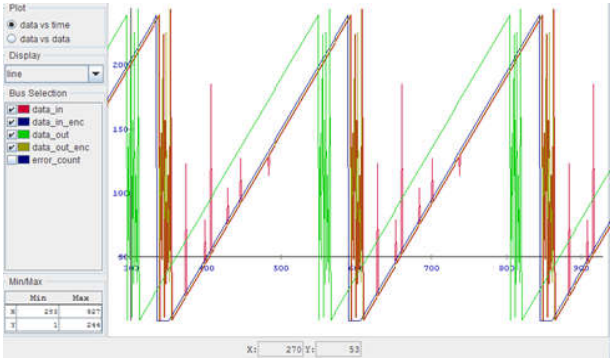

Figure 13 Hardware test results of the RS system

CONCLUSION AND FUTURE SCOPE

RS codes are widely used in Satellite and Deep Space Commutations, CD / DVD Drives, Large Memory Devices, Complex TDM/FDM system in Defense Equipment.

The design of the encoder/decoder was described in VHDL by carrying functional simulation using ModelSim 10.1c and validated on FPGA (type FF1156-1LX240T and XC3E-5FG320) using the software Xilinx Integrated Design Environment 13.1. The results showed that the area occupied and the latency is very convincing. The Configurable latency about 2^m – 2*(n-k) clock cycles is an overhead. Indeed, we have achieved re-configurability by adopting architecture in which each block is pipeline and/or parallelized.

The code is Configurable for M values of 6, 7 and 8 i.e, Block length of 64(minimum) and 256(maximum) symbols can undergo RS Decoding of Error correcting capability 12 (minimum) and 16(Maximum) symbols per block. The present Implemented system can be extended for other ‘m’ values up to 16 which is block length 65535 symbols and shorting of codes can also be achieved.

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